EE 330

Lecture 34

Layout of Current Mirrors

Common-Centroid Layouts

High Gain Amplifiers

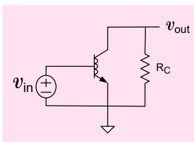
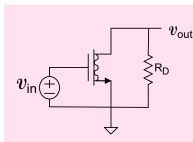
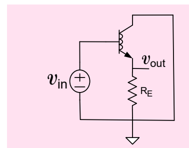
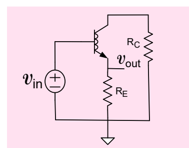
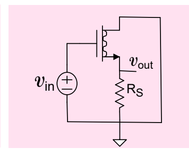
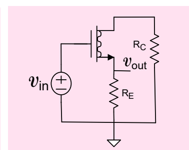
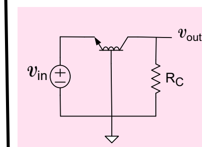
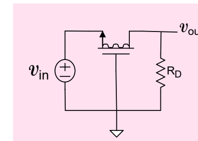
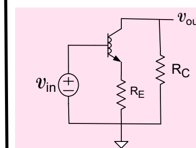
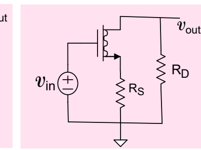
Cascode Amplifiers

Fall 2024 Exam Schedule

Exam 1	Friday	Sept 27
Exam 2	Friday	October 25
Exam 3	Friday	Nov 22
Final Exam	Monday	Dec 16 12:00 - 2:00 PM

Review From Previous Lecture

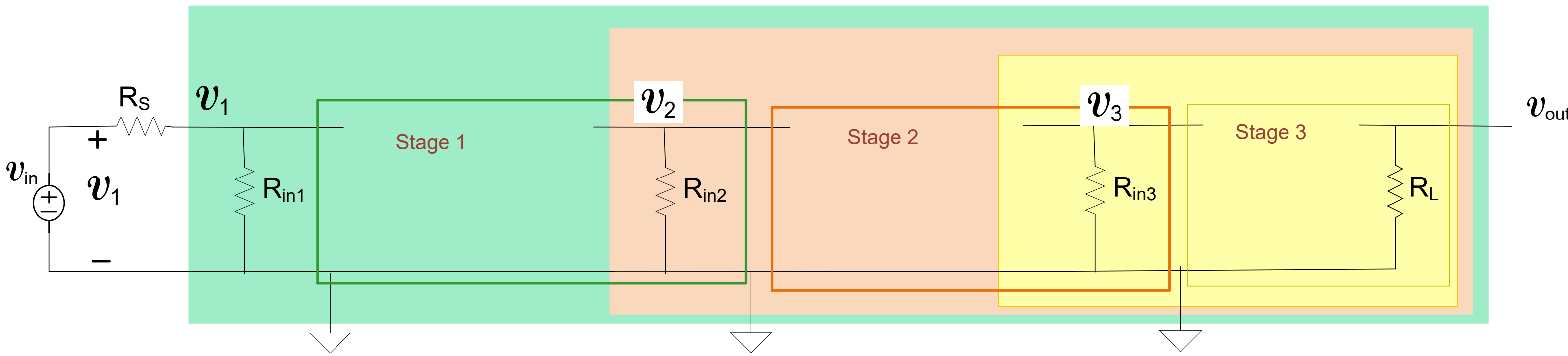
Basic Amplifier Application Gain Table

	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
			 	 				
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E}$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi+\beta R_E$		g_m^{-1}		$r_\pi+\beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

(not two-port models for the four structures)

Can use these equations only when small signal circuit is EXACTLY like that shown !!

Formalization of cascade circuit analysis working from load to input: (when stages are unilateral or not unilateral)



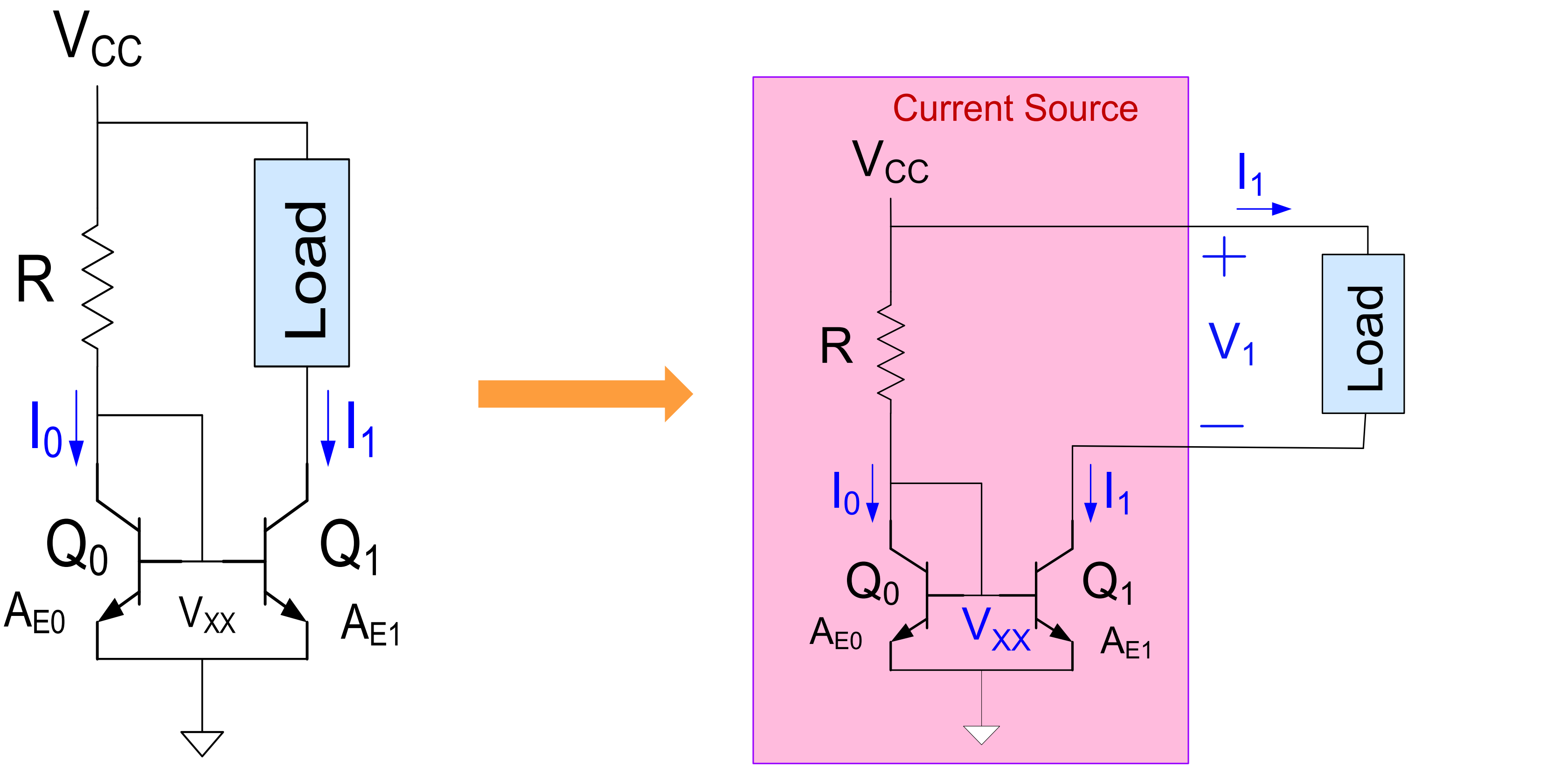
R_{ink} includes effects of all loading
Must recalculate if any change in loading
Analysis systematic and rather simple

$$\frac{v_{OUT}}{v_{IN}} = \frac{v_1}{v_{IN}} \frac{v_2}{v_1} \frac{v_3}{v_2} \frac{v_{OUT}}{v_3}$$

This was the approach used in analyzing the previous cascaded amplifier

Current Sources/Mirrors

Will show circuit in red behaves as a current source



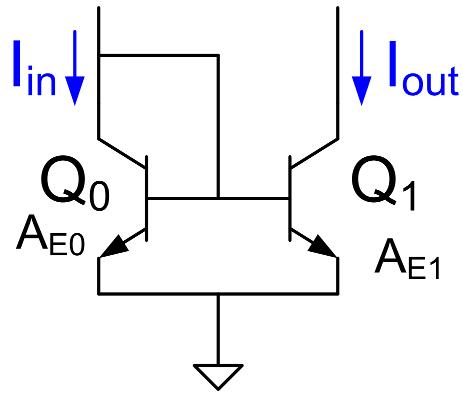
R and Q_0 simply generate voltage V_{XX} in previous circuit

But sensitivity of I_1 is much smaller than using voltage source for generating V_{XX}

Summary of Missing Material from Lecture 33

Start Here:

Current Sources/Mirrors



npn Current Mirror

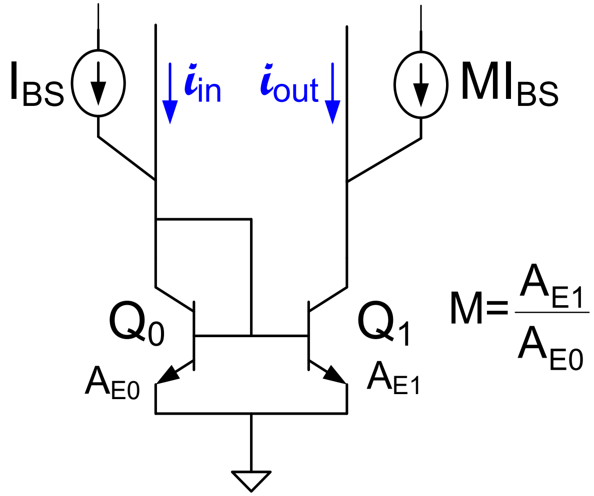
If the base currents are neglected

$$I_{out} = \left[\frac{A_{E1}}{A_{E0}} \right] I_{in}$$

- **Output current linearly dependent on I_{in}**
- **Small-signal and large-signal relationships the same since linear**
- **Serves as a current amplifier**
- **Widely used circuit**

But I_{in} must be positive !

Current Sources/Mirrors



npn current mirror amplifier

i_{out}=?

$$\frac{i_{OUT}+MI_{BS}}{i_{in}+I_{BS}}=M$$

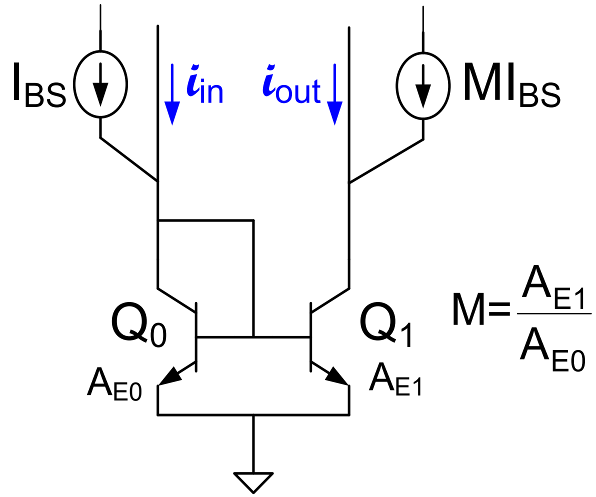
$$i_{OUT}+MI_{BS}=M\left(i_{in}+I_{BS}\right)$$

$$i_{OUT}+M\cancel{I}_{BS}=M\left(i_{in}+\cancel{I}_{BS}\right)$$

$$\frac{i_{OUT}}{i_{in}}=M$$

But $I_{BS}+i_{in}>0$!

Current Sources/Mirrors



npn current mirror amplifier

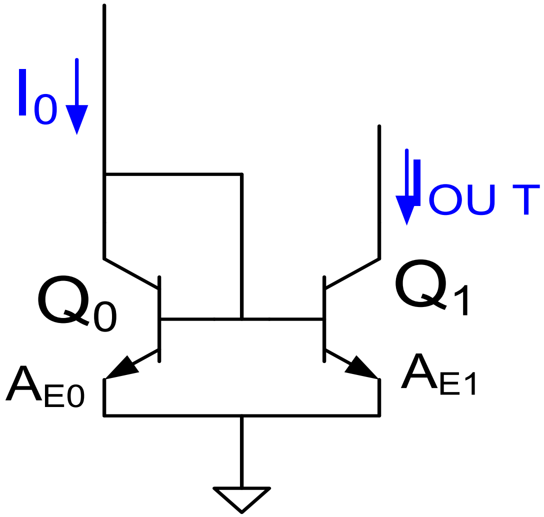
$$i_{out} = \left[\frac{A_{E1}}{A_{E0}}\right] i_{in}$$

Amplifies both positive and negative currents (provided $i_{IN} > -I_{BS}$)

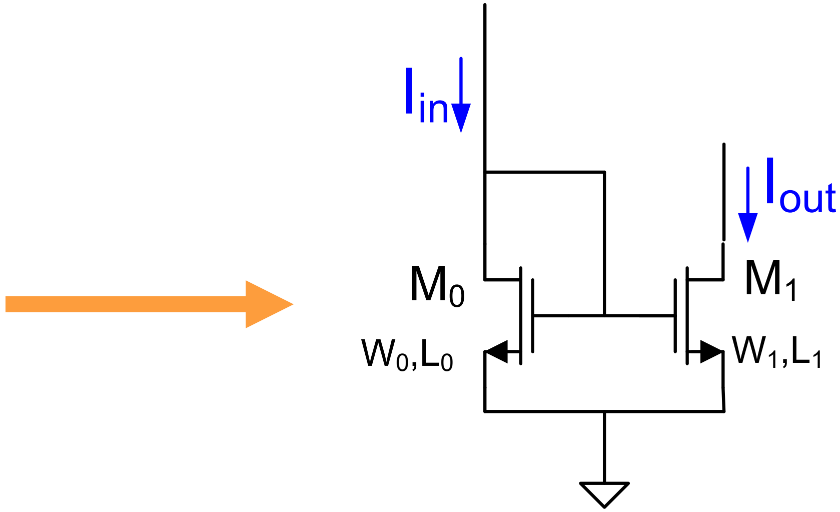
Current amplifiers are easy to build !!

Current gain can be accurately controlled with appropriate layout !!

Current Sources/Mirrors



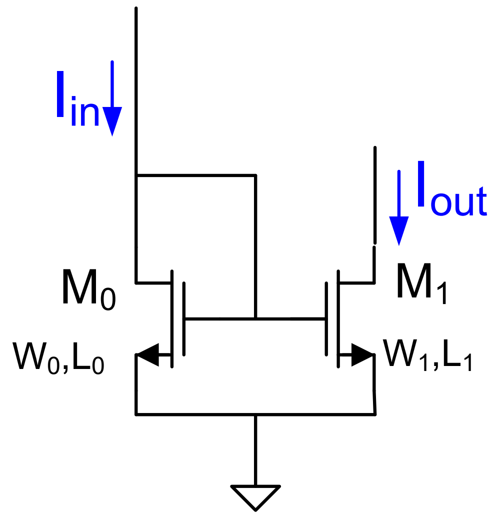
npn Current Mirror



n-channel Current Mirror

I_{out}=?

Current Sources/Mirrors



n-channel Current Mirror

$$I_{in} = \frac{\mu C_{OX} W_0}{2L_0}\left(V_{GS0} - V_{T0}\right)^2$$

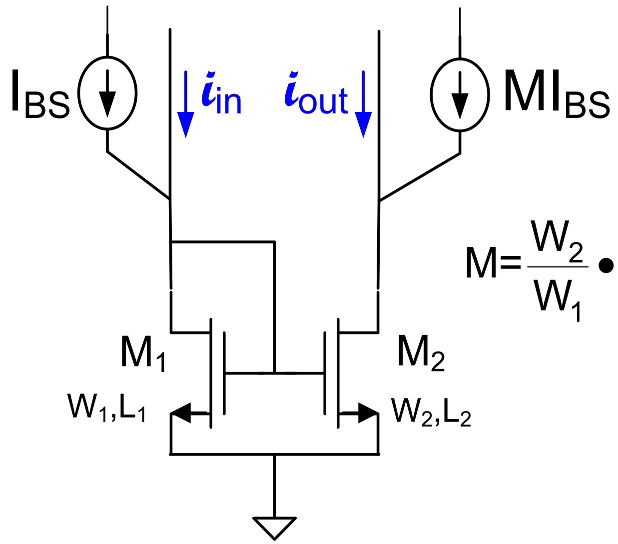
$$I_{out} = \frac{\mu\, C_{OX} W_1}{2L_1}\left(V_{GS1} - V_{T1}\right)^2$$

If process parameters are matched, it follows that

$$I_{out} = \left[\frac{W_1}{W_0}\frac{L_0}{L_1}\right] I_{in}$$

- Current mirror gain can be accurately controlled !
- Layout is important to get accurate gain (for both MOS and BJT)

n-channel current mirror current amplifier

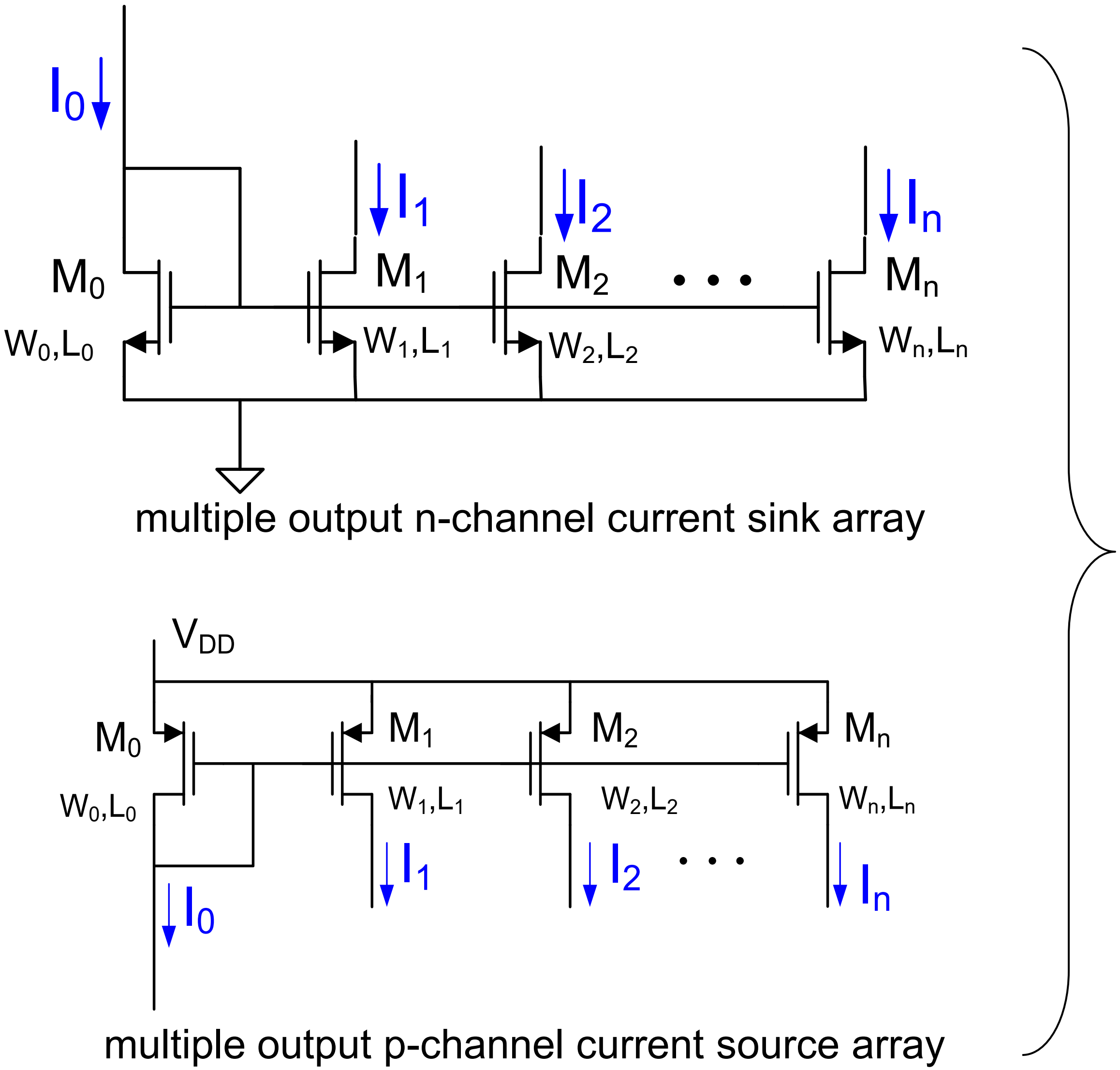


$$M=\frac{W_2}{W_1}\bullet\frac{L_1}{L_2}$$

$$i_{out}=\left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]i_{in}$$

Amplifies both positive and negative currents

Current Sources/Mirrors



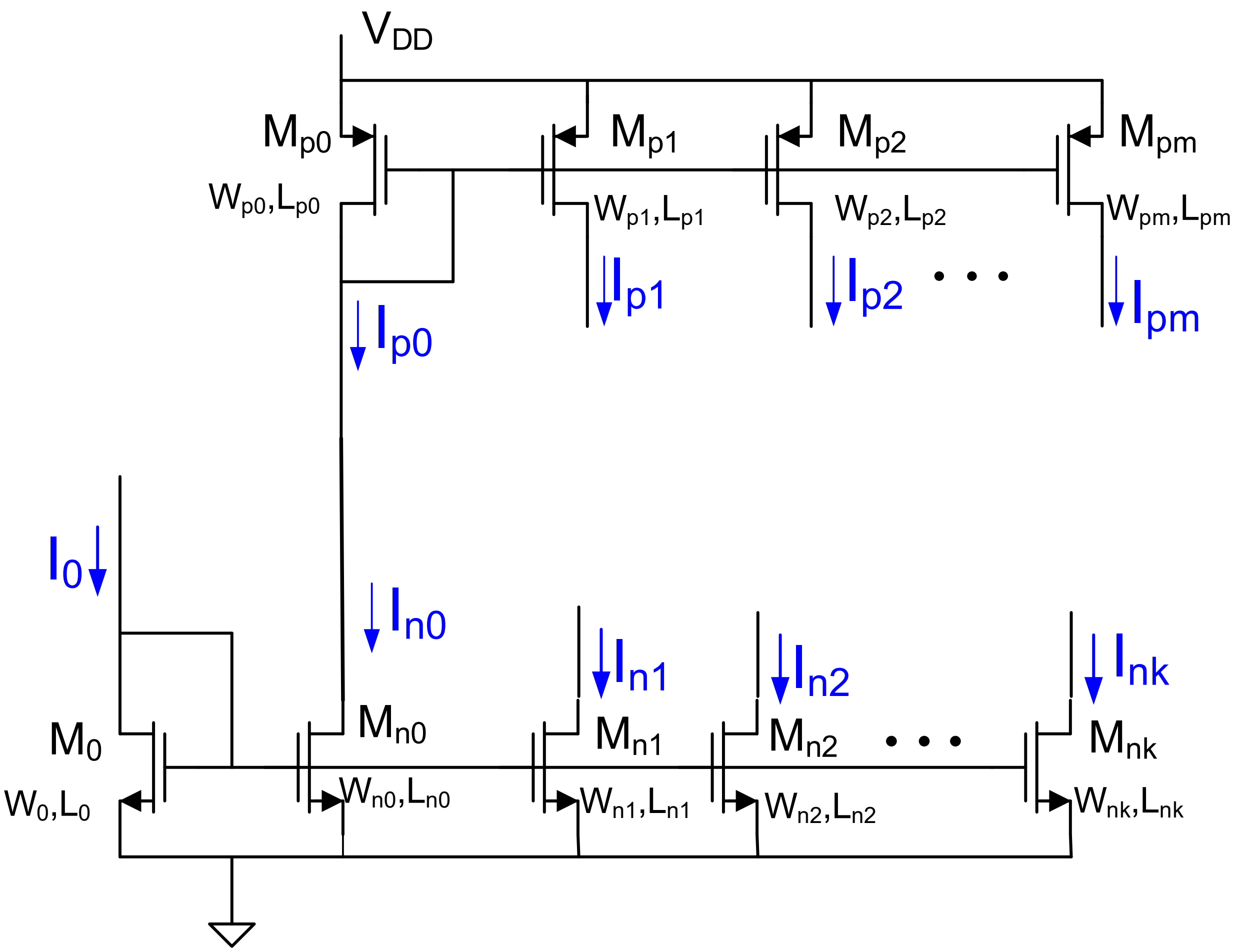
multiple output n-channel current sink array

multiple output p-channel current source array

$$I_k = \left[\frac{W_k}{W_0} \frac{L_0}{L_k} \right] I_0$$

Current Sources/Mirrors

multiple sourcing and sinking current outputs



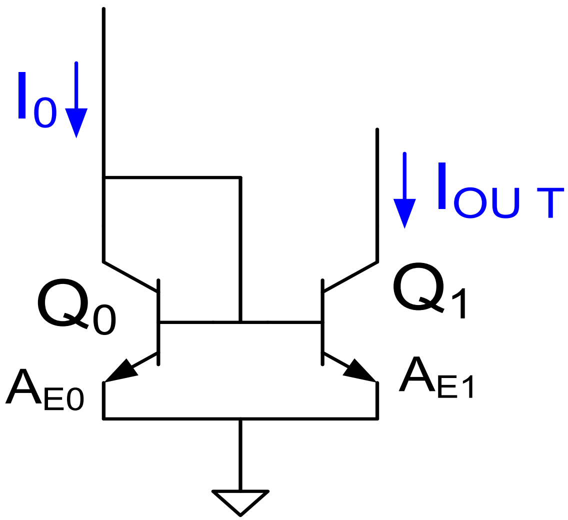
$$I_{pj}=\left[\frac{W_{pj}}{L_{pj}}\bullet\frac{L_{p0}}{W_{p0}}\right]MI_0$$

$$M=\left[\frac{W_{n0}}{L_{n0j}}\bullet\frac{L_0}{W_0}\right]$$

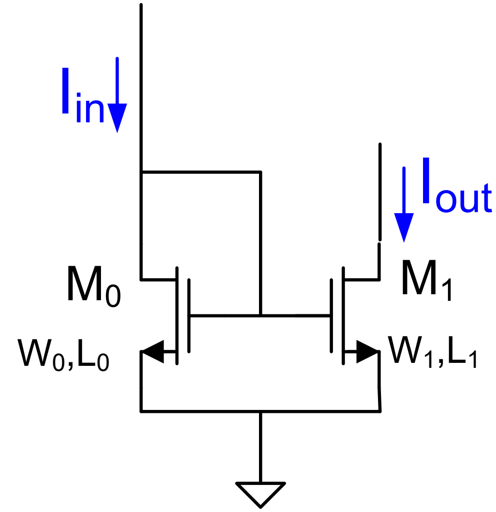
$$I_{nj}=\left[\frac{W_{nj}}{L_{nj}}\bullet\frac{L_0}{W_0}\right]I_0$$

m and k may be different
Often M=1

Current Sources/Mirrors Summary



npn Current Mirror



n-channel Current Mirror

$$I_{out} = \left[\frac{A_{E1}}{A_{E0}} \right] I_{in}$$

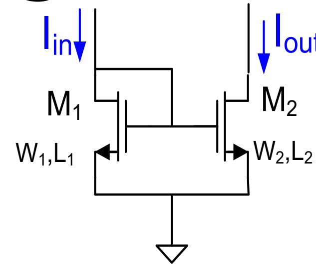
$$I_{out} = \left[\frac{W_1}{W_0} \frac{L_0}{L_1} \right] I_{in}$$

- Current mirror gain can be accurately controlled !
- Layout is important to get accurate gain (for both MOS and BJT)

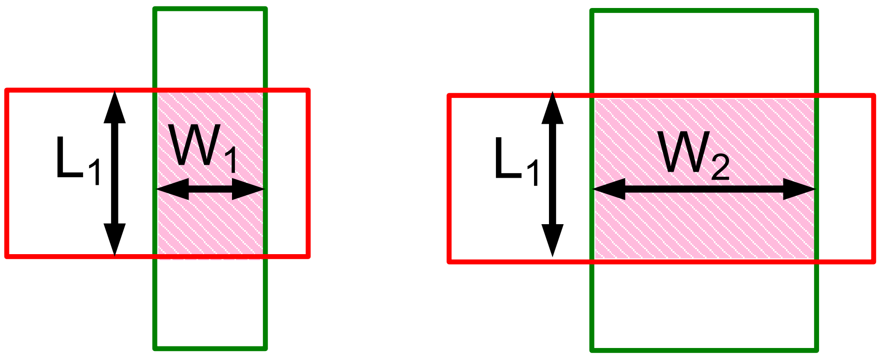
Summary of Missing Material from Lecture 33

End Here:

Layout of Current Mirrors

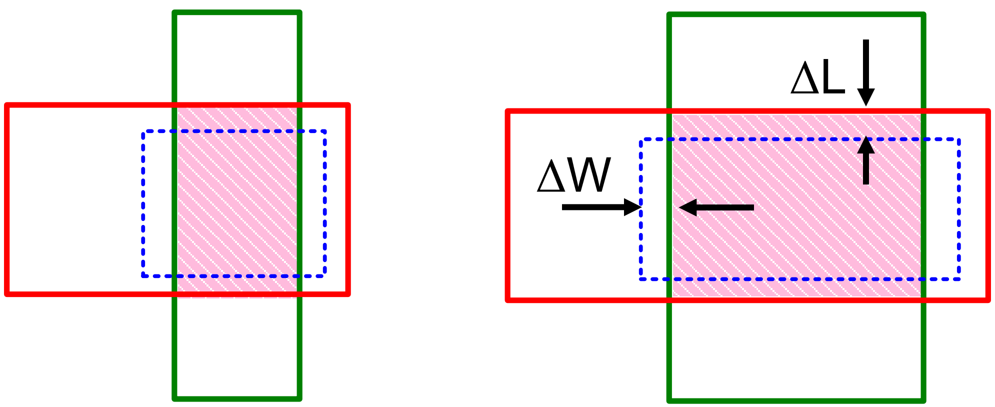


Example with M = 2



$$M=\left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]$$

Standard layout



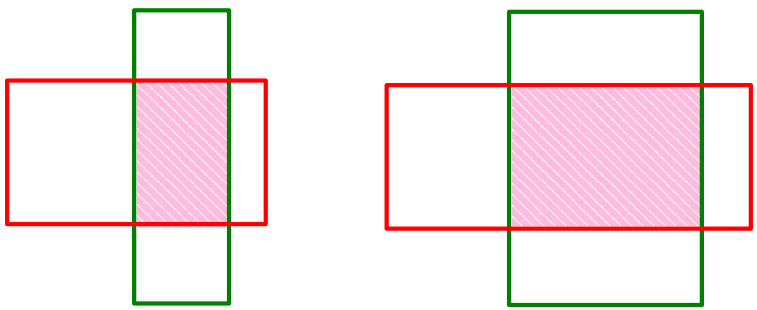
$$M=\left[\frac{W_2+2\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_2+2\Delta L}\right]$$

$$M=\left[\frac{2W_1+2\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]\neq 2$$

Gate area after fabrication depicted

Layout of Current Mirrors

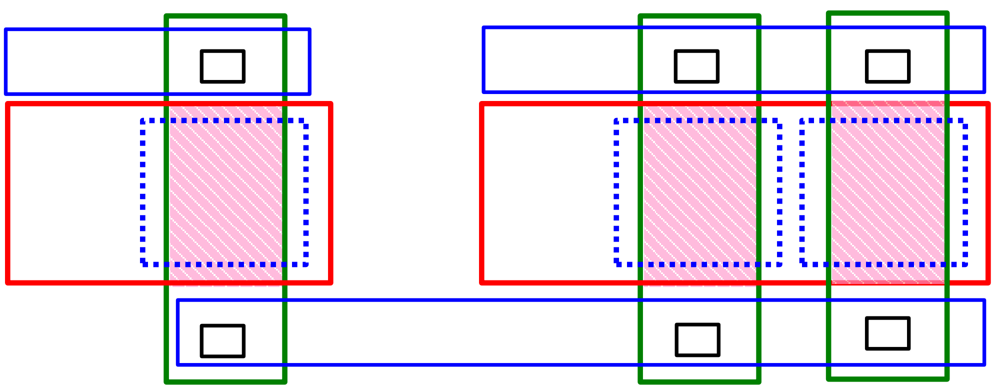
Example with M = 2



$$M = \left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]$$

$$M = \left[\frac{2W_1 + 2\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L}\right] \neq 2$$

Standard layout



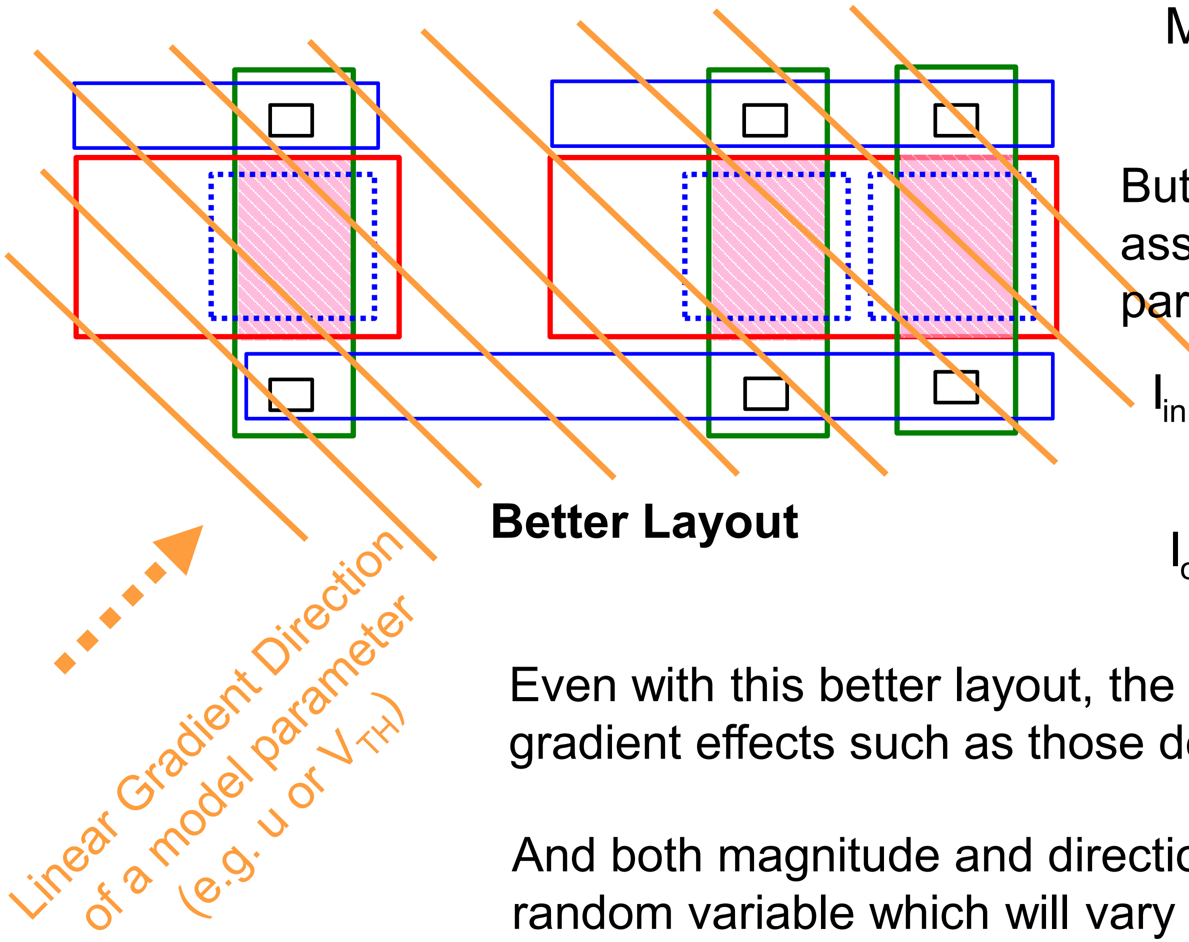
$$M = \left[\frac{2W_1 + 4\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L}\right] = 2$$

Better Layout

Layout of Current Mirrors

Example with M = 2

$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$



Better Layout

But this analysis was based upon assumption of matching of process parameters

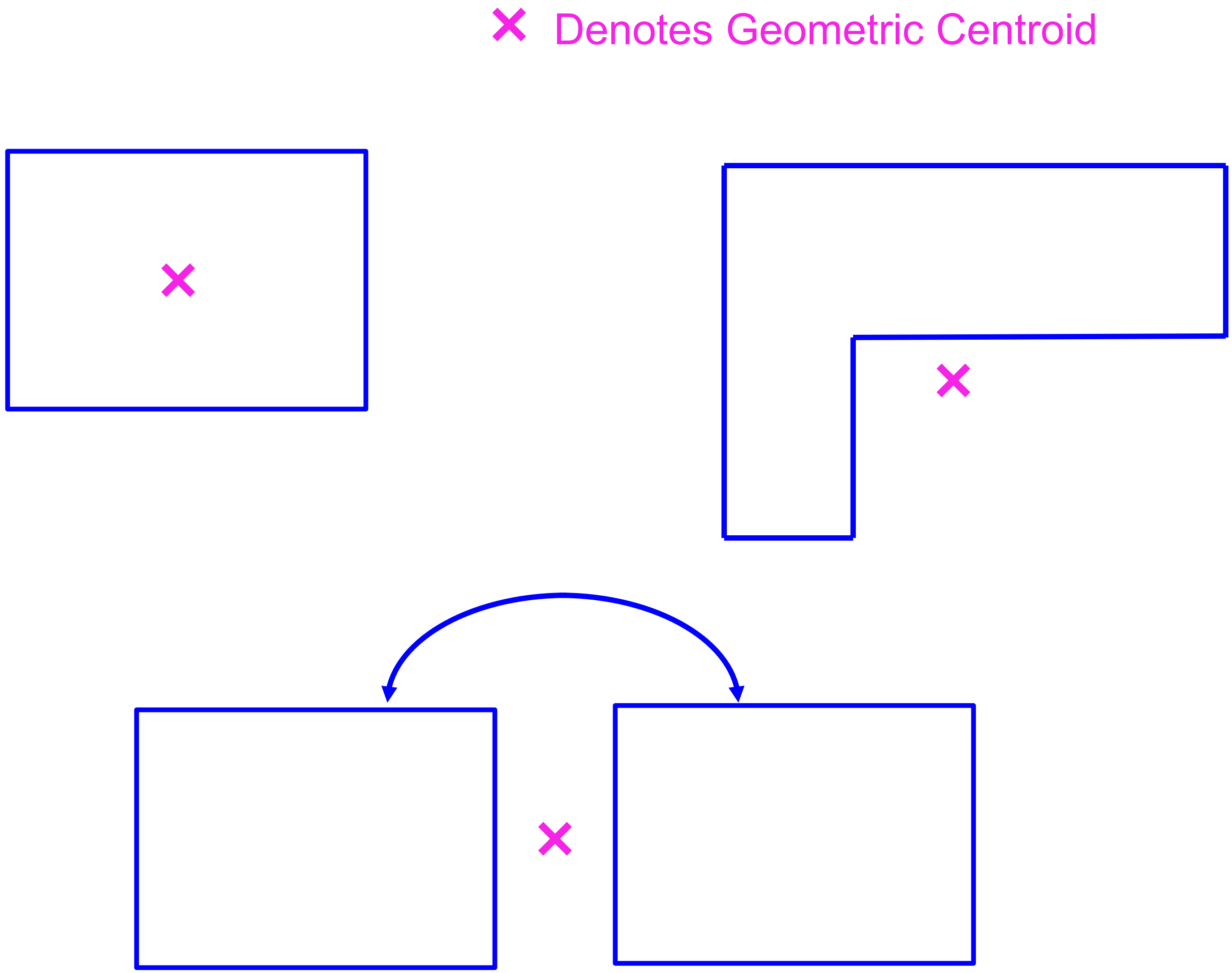
$$I_{in}=\frac{\mu_0 C_{OX} W_0}{2L_0}\left(V_{GS0}-V_{T0}\right)^2$$

$$I_{out}=\frac{\mu_1 C_{OX} W_1}{2L_1}\left(V_{GS1}-V_{T1}\right)^2$$

Even with this better layout, the current ratio will not be 2 if gradient effects such as those depicted here are shown

And both magnitude and direction of gradient effects are a random variable which will vary across a die

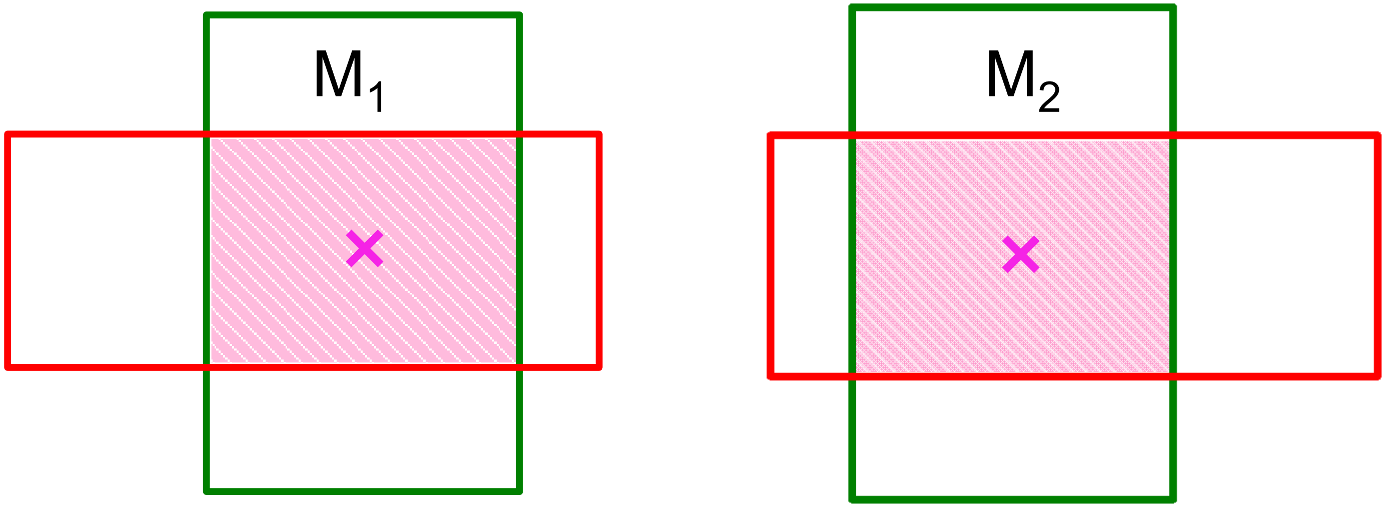
Centroid and Common Centroid



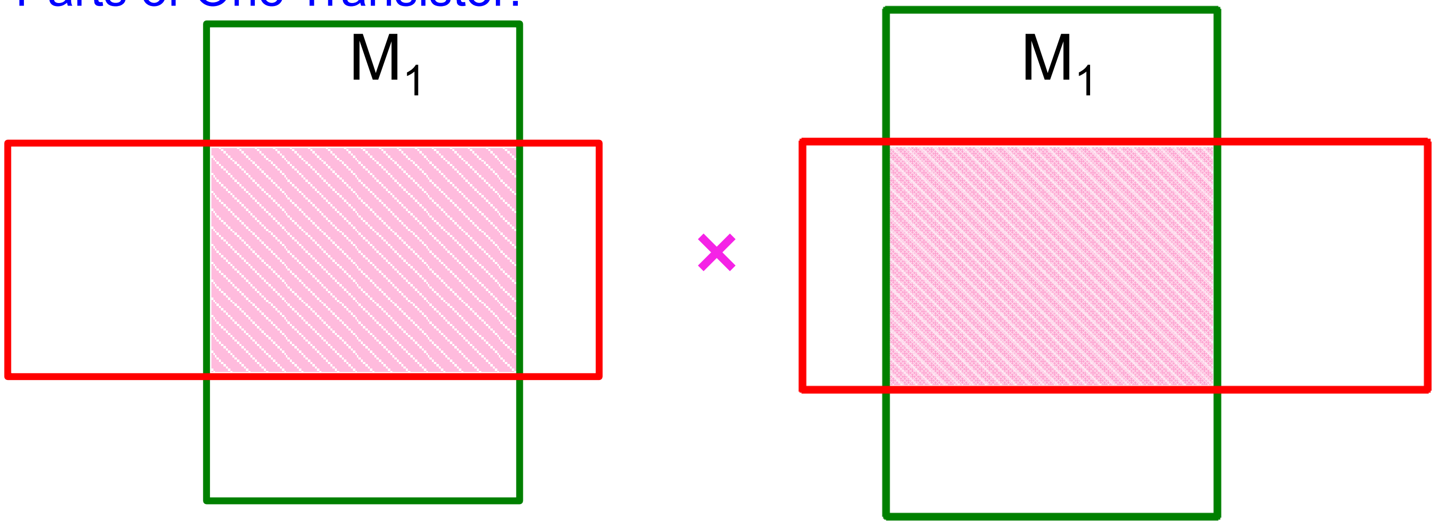
Centroid and Common Centroid

Geometric Centroids of Channel

Two Transistors:

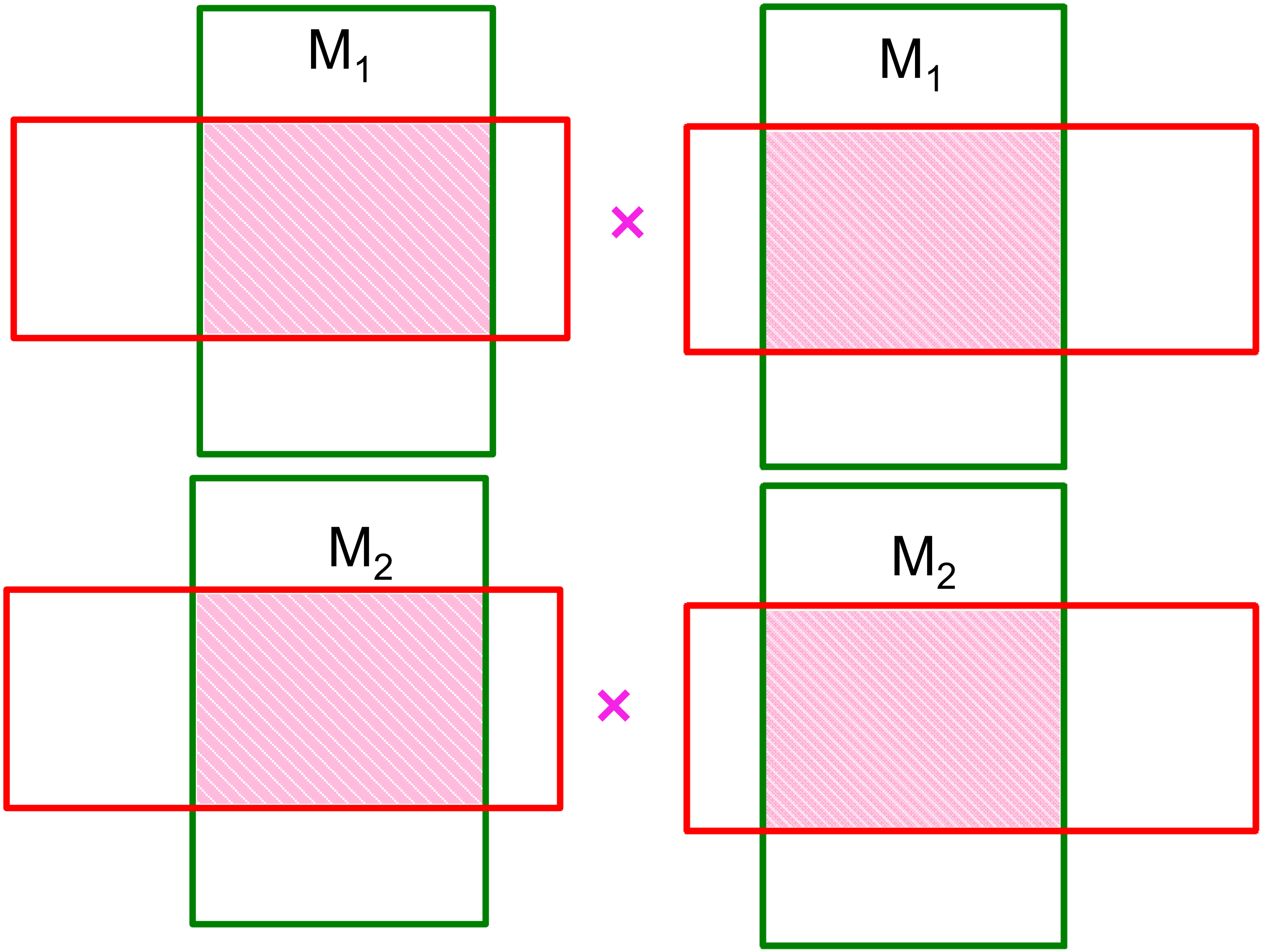


Two Parts of One Transistor:



Centroid and Common Centroid

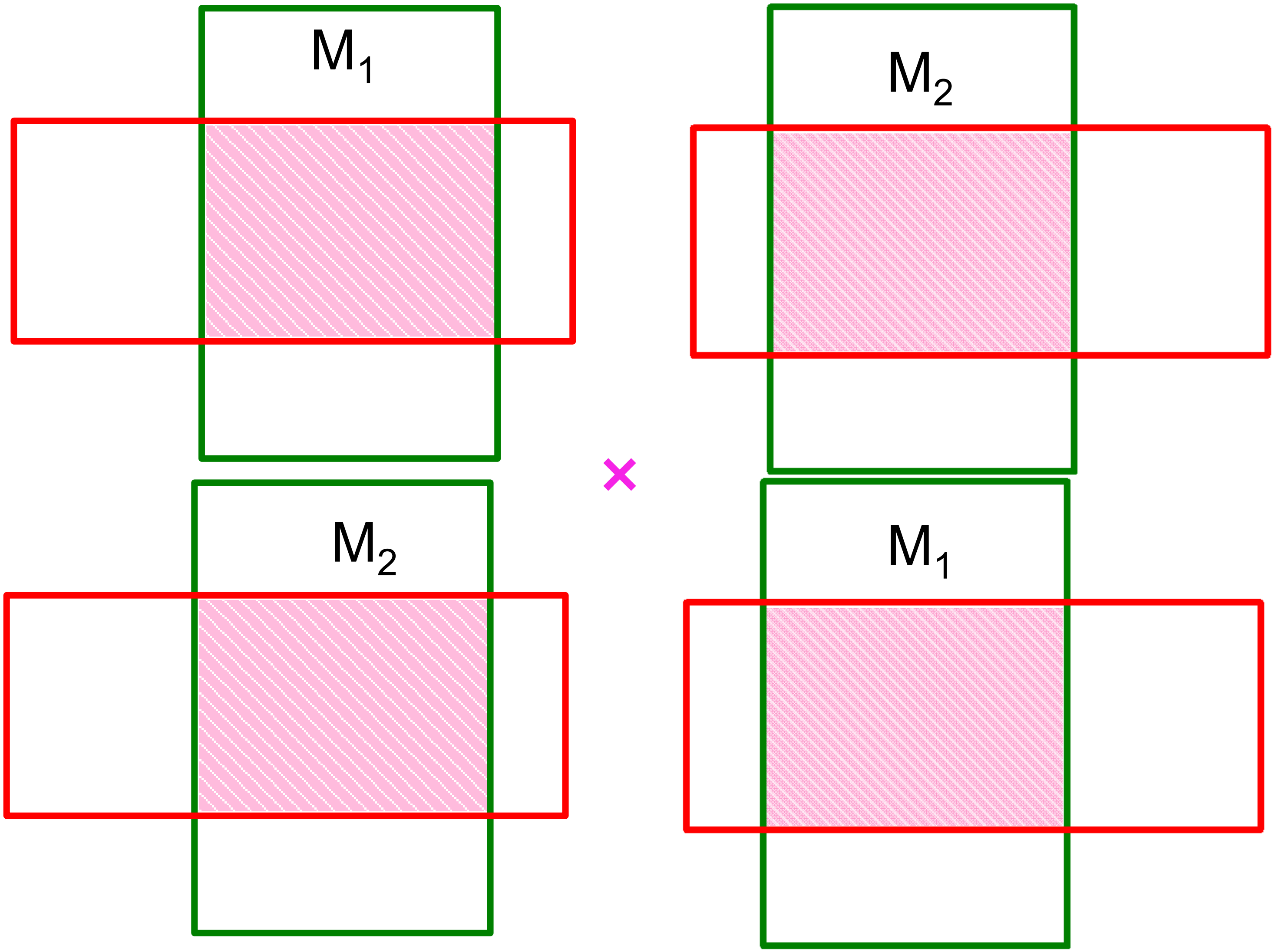
Two Transistors each with two parts:



Centroid and Common Centroid

Common Centroid for Ideally Matched Devices

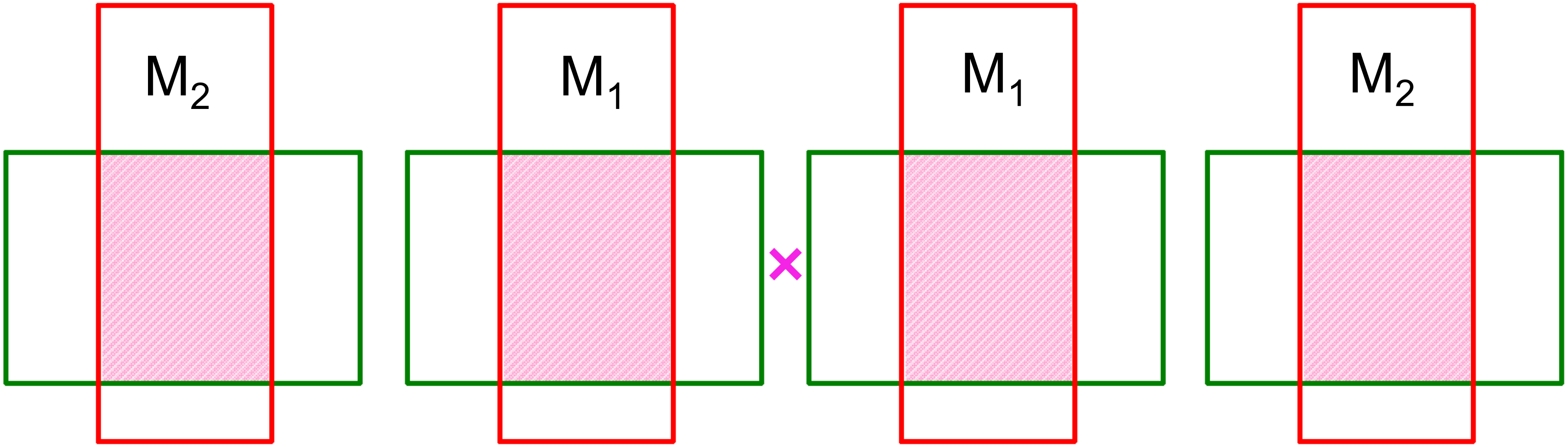
Two Transistors each with two parts:



Centroid and Common Centroid

Common Centroid for Matched Devices

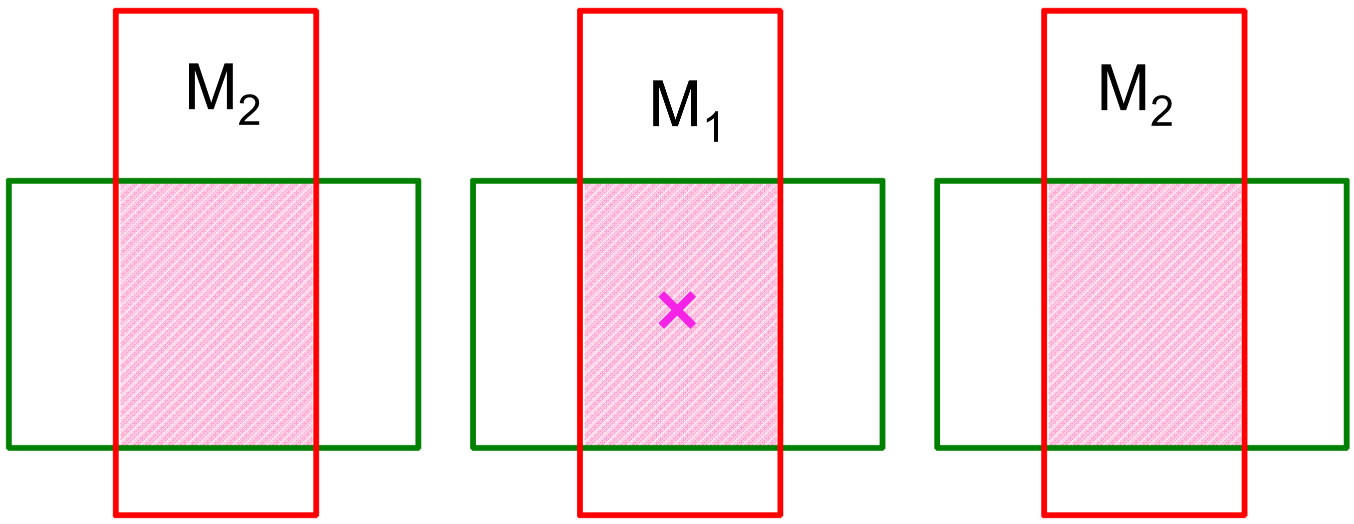
Two Transistors each with two parts:



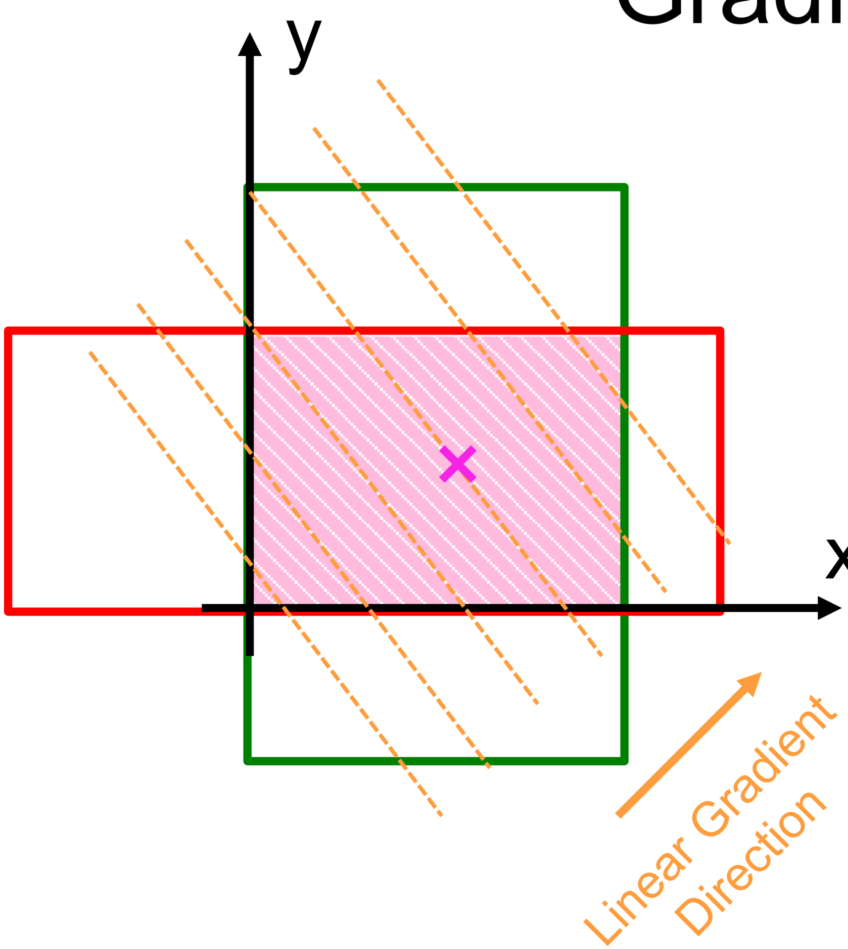
Centroid and Common Centroid

Common Centroid for Ratioed Devices $M = \frac{W_2}{W_1}\frac{L_1}{L_2} = 2$

Two Transistors with different effective widths:



Gradient



Threshold voltage dependent upon position

$V_{TH}(x,y)$

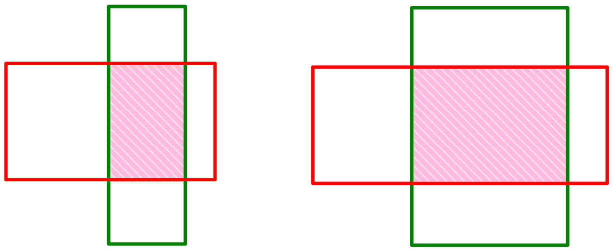
- Significant changes in threshold voltage can occur due to gradient effects
- This can seriously degrade matching in matching-critical circuits

- If the threshold voltage of a transistor changes with position, it can be reasonably accurately modeled with an "equivalent" threshold voltage
- For linear gradient, $V_{THEQ}=V_{TH}(X_C,Y_C)$

× : (X_C,Y_C)

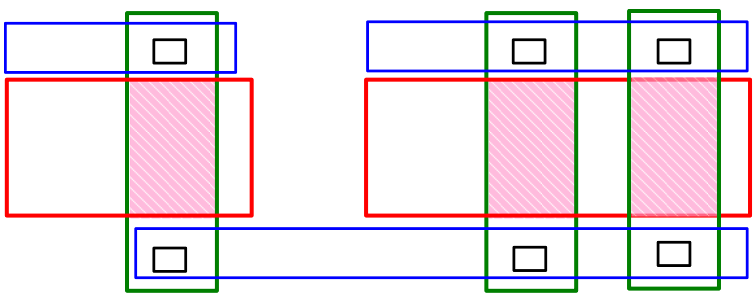
Layout of Current Mirrors

Example with M = 2



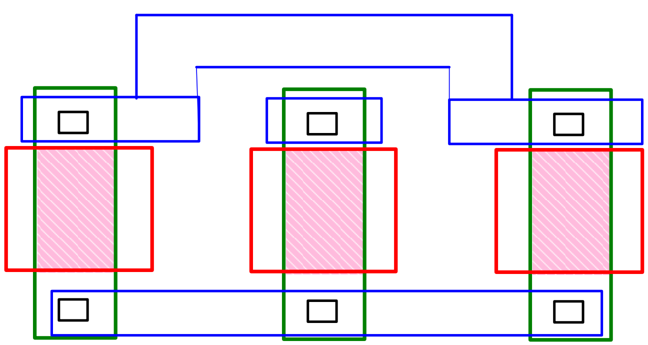
Standard layout

$$M=\left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]$$



Better Layout

$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$

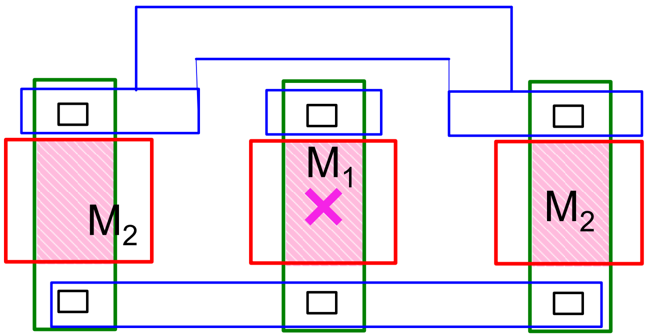


Even Better Layout

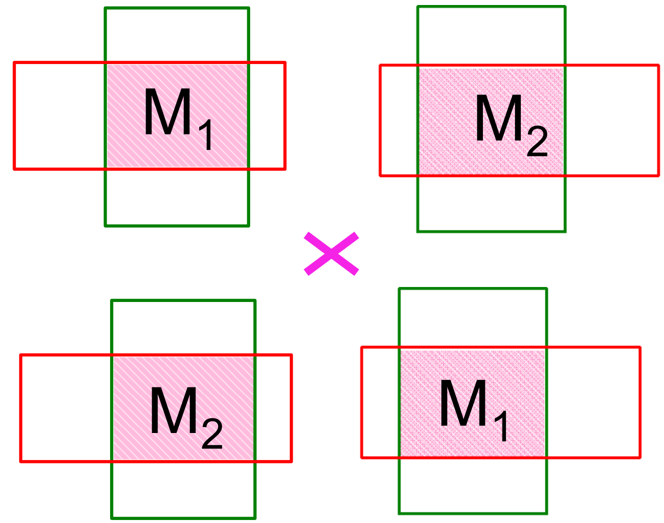
$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$

- **This is termed a common-centroid layout**
- **Linear gradient mismatch eliminated with common-centroid layout !**

Common-Centroid Layouts



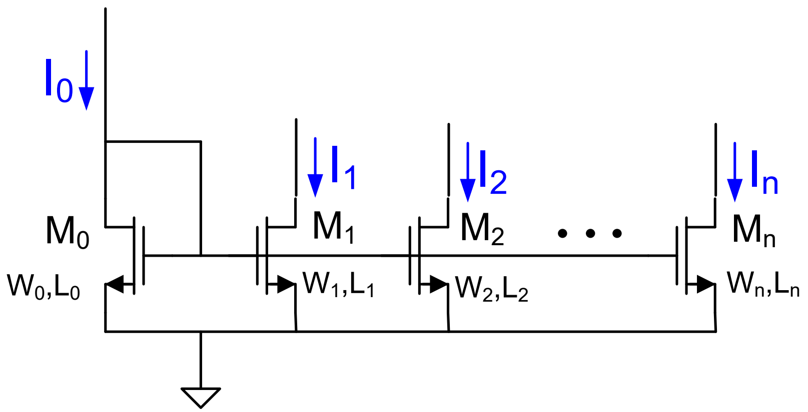
$$M=\left[\frac{2W_1}{W_1}\bullet\frac{L_1}{L_1}\right]=2$$

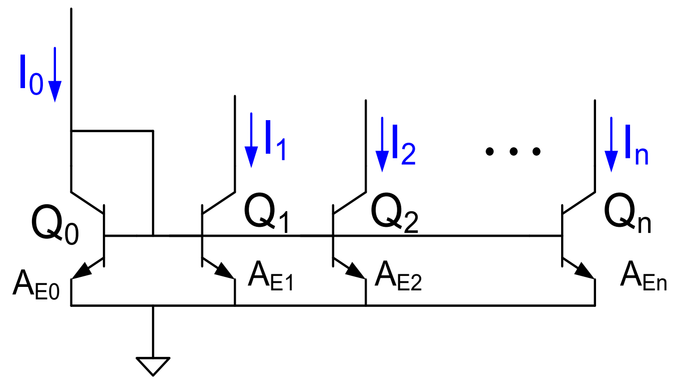


$$M=\left[\frac{2W_1}{2W_1}\bullet\frac{L_1}{L_1}\right]=1$$

- Individual transistors often decomposed into parallel multiple unary devices connected in parallel
- Common-Centroid layout approach widely used to minimize (ideally cancel) gradient effects in matching-critical circuits
- Applications extend well beyond current mirrors
- More than 2 devices can share a common centroid

Current Sources/Mirrors

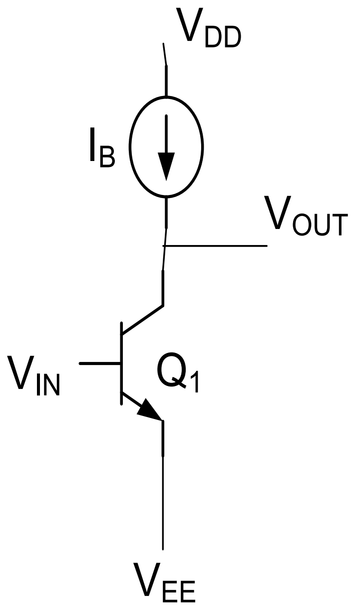




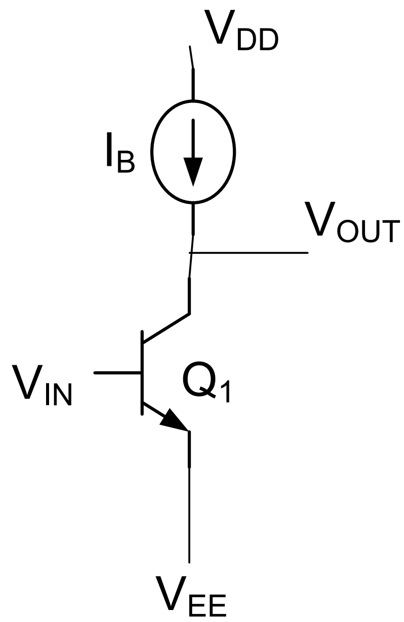
If I_0 is practically generated (it can be), now have available a large number of accurate current sources or sinks that can be used for biasing and for other purposes on chip !

High-gain amplifier

Will now return to discussion of high gain amplifiers



High-gain amplifier



$$A_V \cong -8000$$

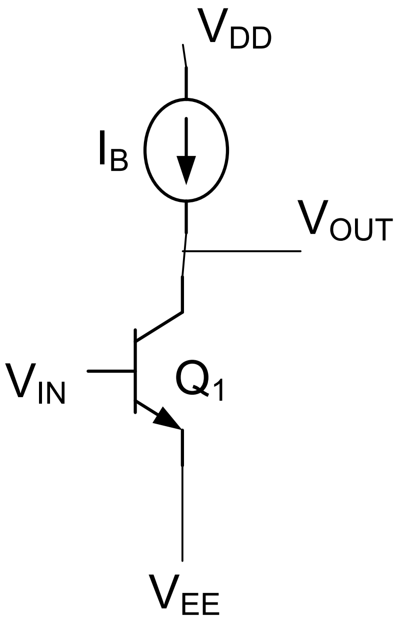
Why are we interested in high-gain amplifiers?

- High gain amplifiers typically have some very undesirable properties

  Nonlinear, gain highly dependent upon process variations and temperature, frequency response poor, noisy, ….

- So we can build feedback amplifiers !!

High-gain amplifier



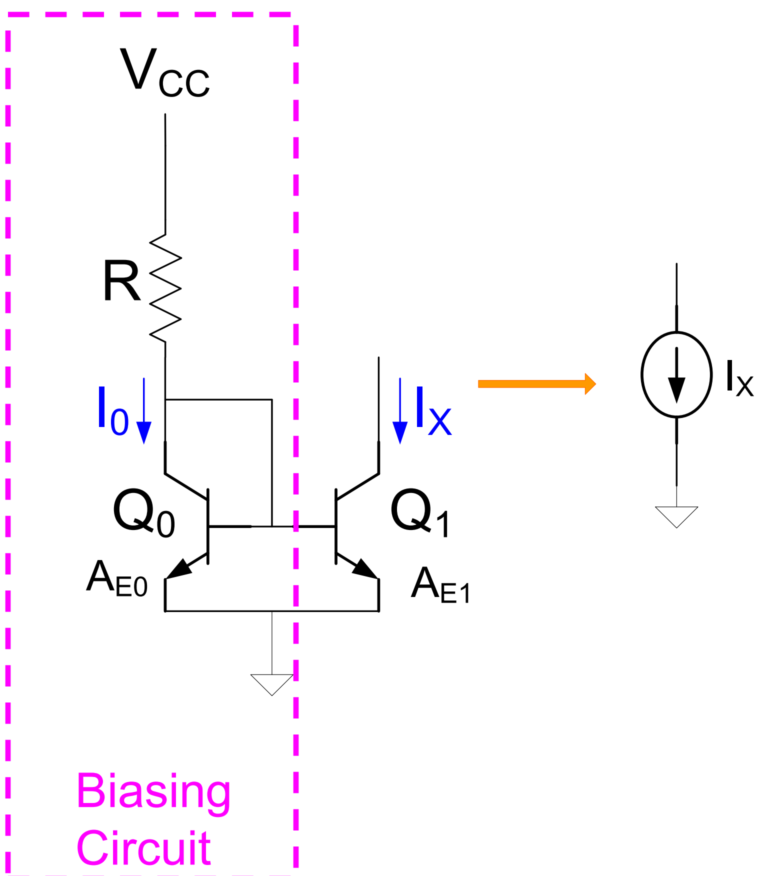
$$A_V \cong -8000$$

→ How can we build the current source?

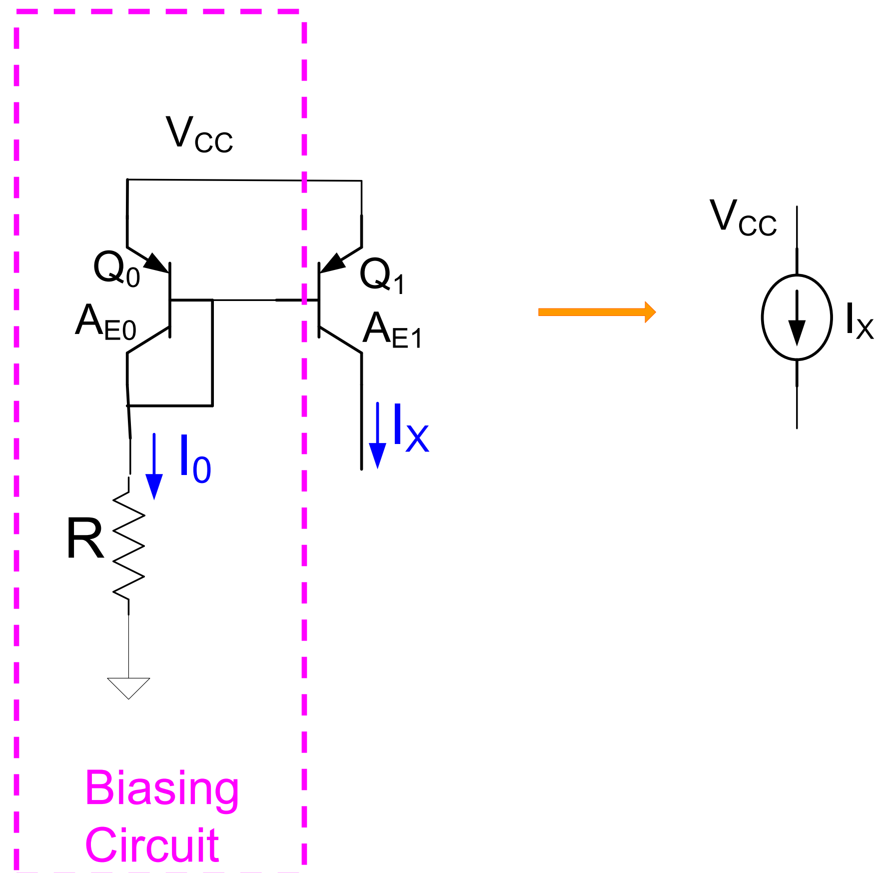
What is the small-signal model of an actual current source?

Basic Current Sources and Sinks

Bipolar Mirror-Based Current Sink

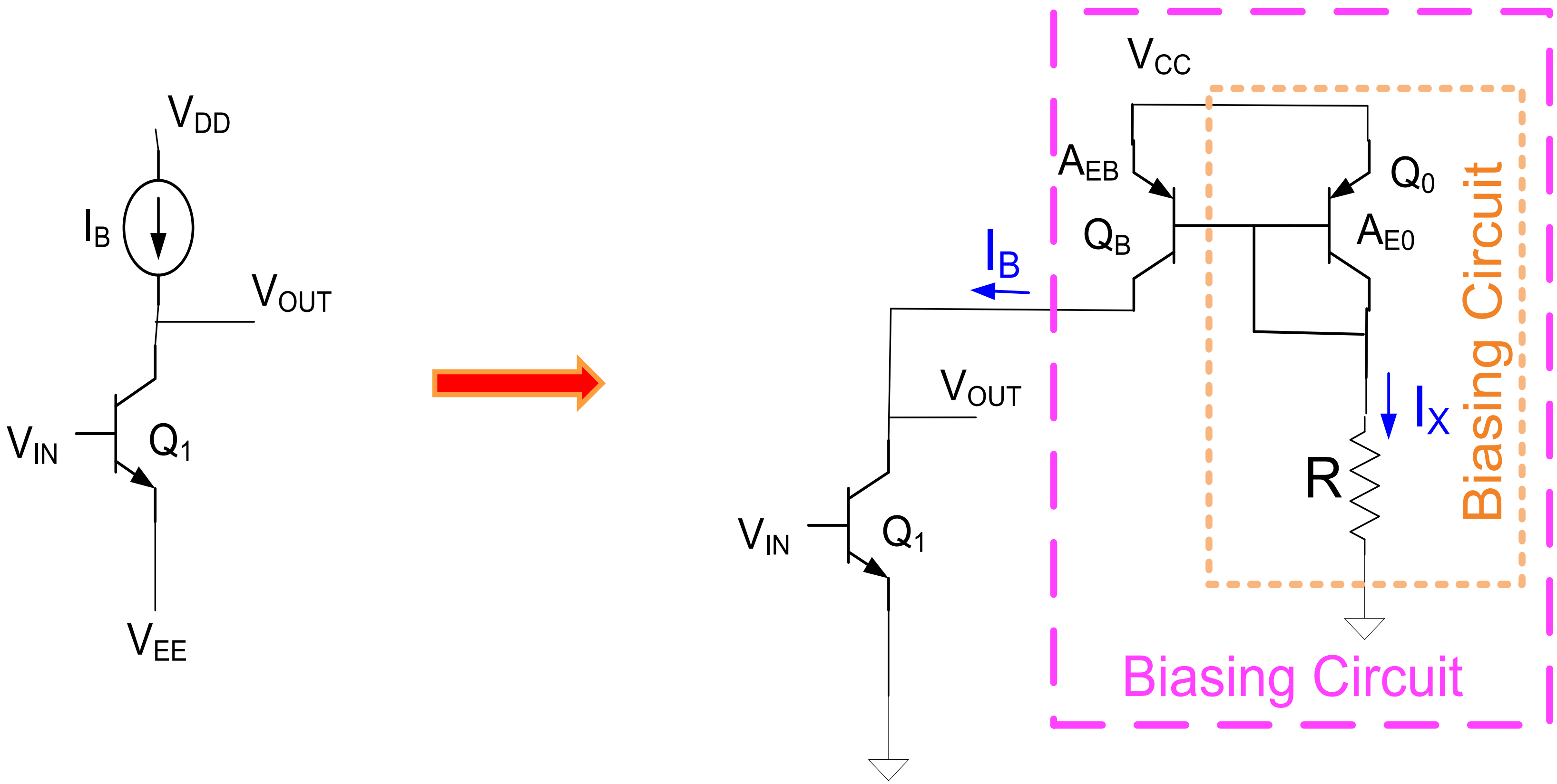


Bipolar Mirror-Based Current Source



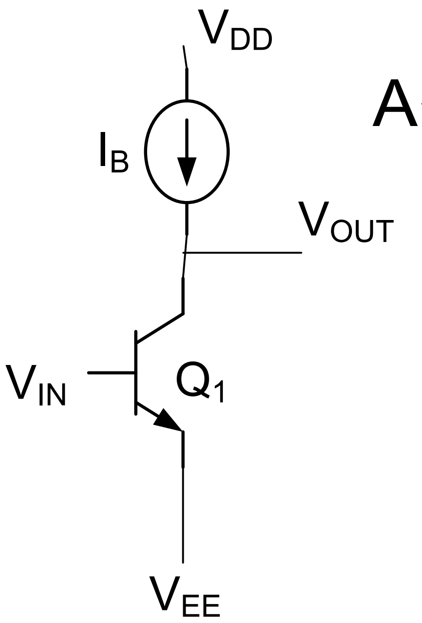
Biasing circuit uses same V_{CC} as amplifier and no other independent sources

High-gain amplifier

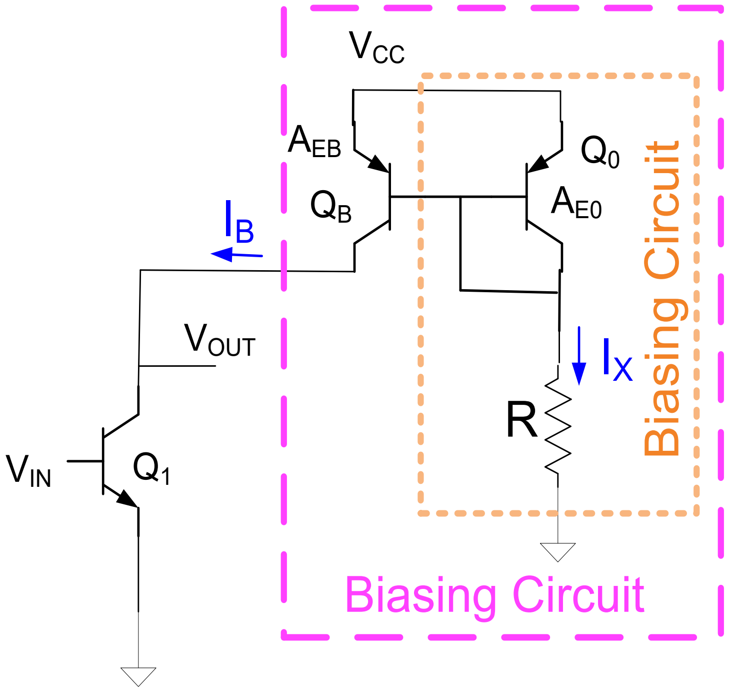


- Bias circuitry requires only a single independent dc voltage source, resistor, and BJT !
- <u>Incremental</u> overhead is only one transistor, Q_B

High-gain amplifier



$$A_V \cong -8000$$



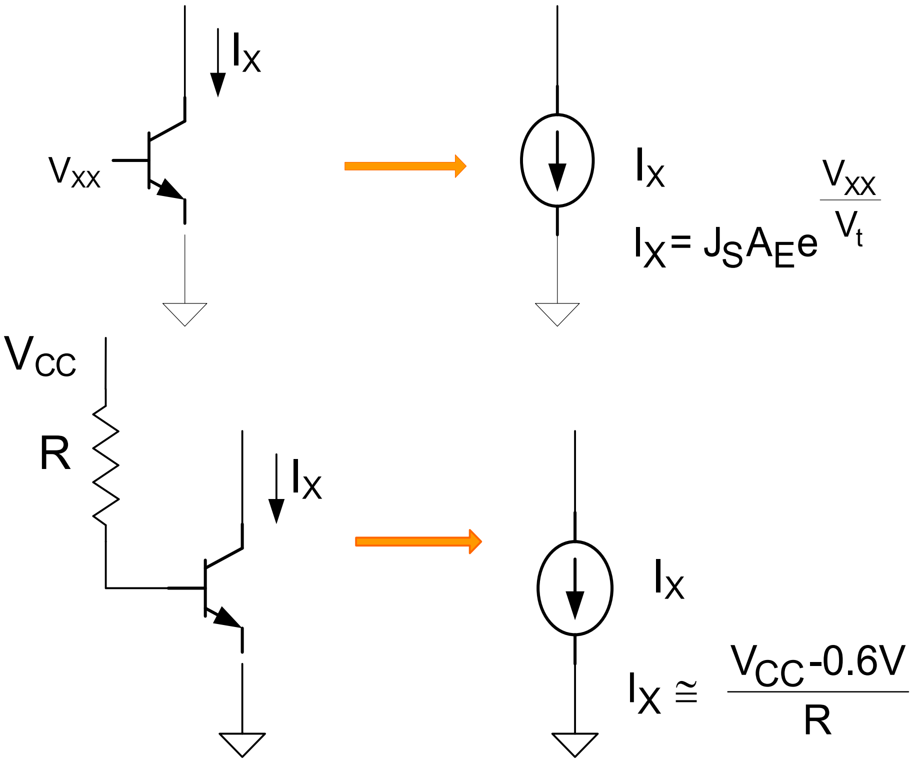
How can we build the current source?

→ What is the small-signal model of an actual current source?

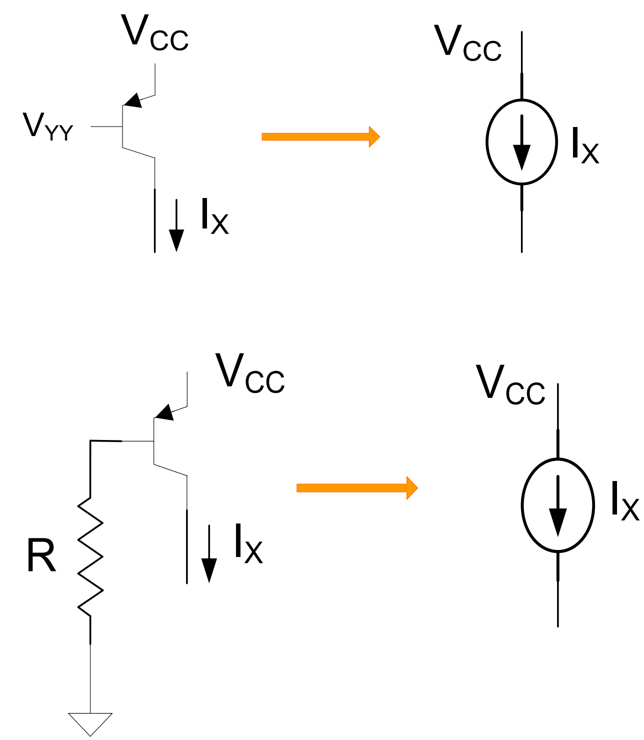
Basic Current Sources and Sinks

What is the small-signal model of an actual current source?

Basic Bipolar Current Sinks



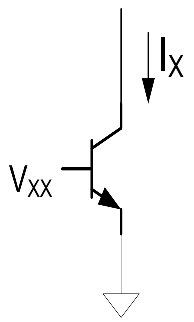
Basic Bipolar Current Sources

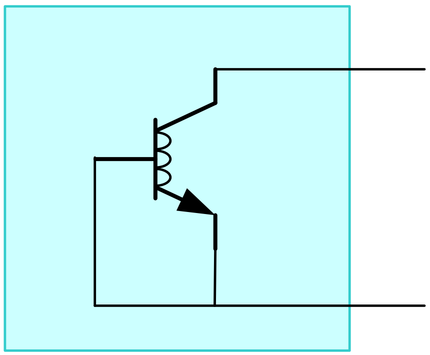


- Very practical methods for biasing the BJTs (or MOSFETs) can be used
- Current Mirrors often used for generating sourcing and sinking currents
- Can think of biasing transistors with V_{XX} and V_{YY} in these current sources

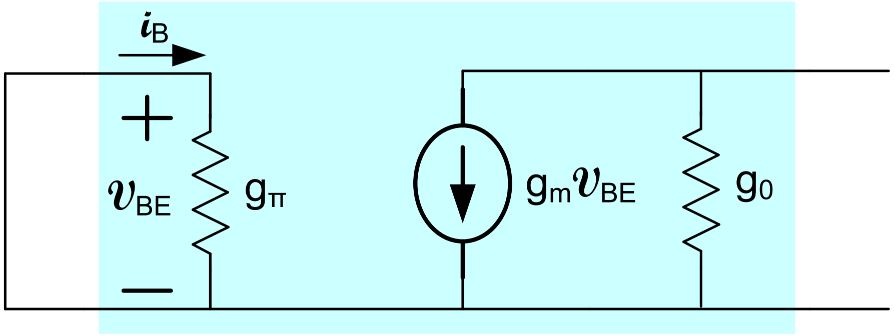
Basic Current Sources and Sinks

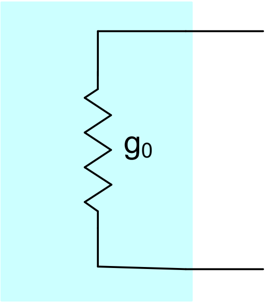
Small-signal Model of BJT Current Sinks and Sources





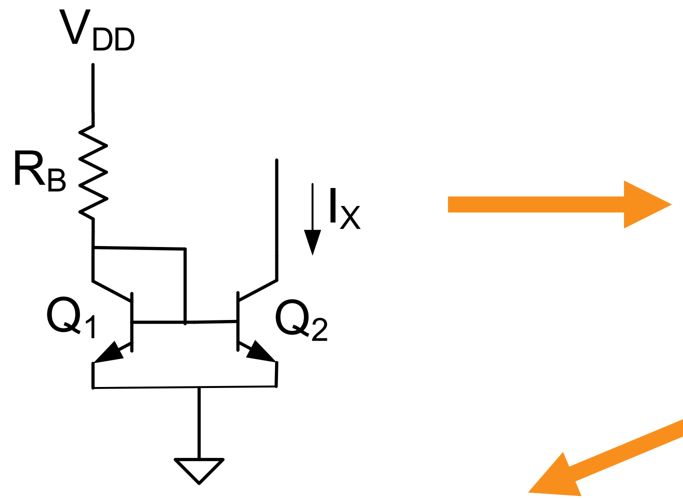
Small-signal BE-Connected
(Not Diode Connected !)

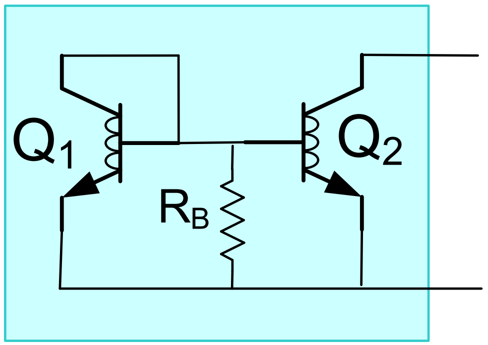




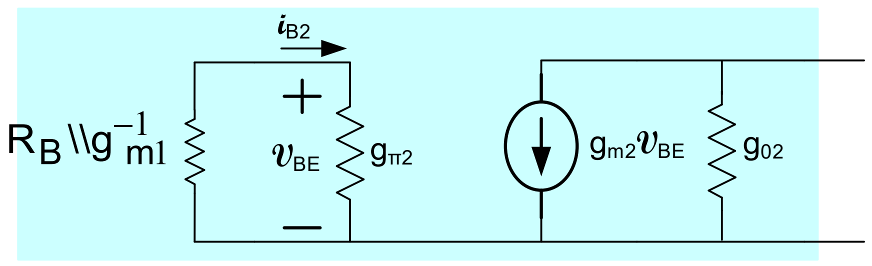
Basic Current Sources and Sinks

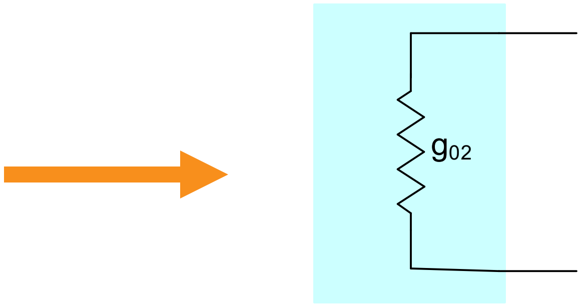
Small-signal Model of BJT Current Sinks and Sources





Small-signal of Q_1
Diode connected

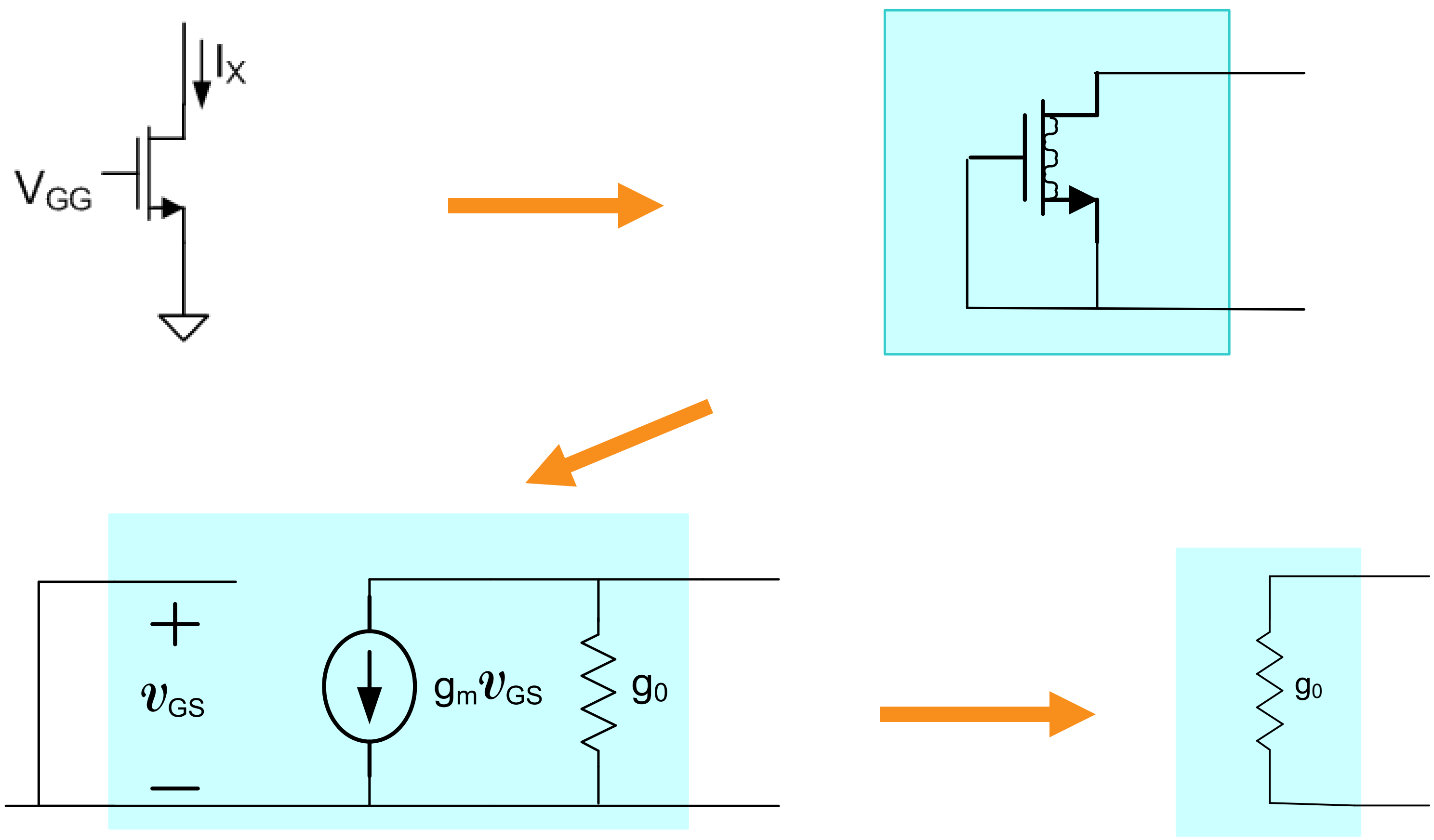




Small-signal model of all other BJT Sinks and Sources introduced so far are the same

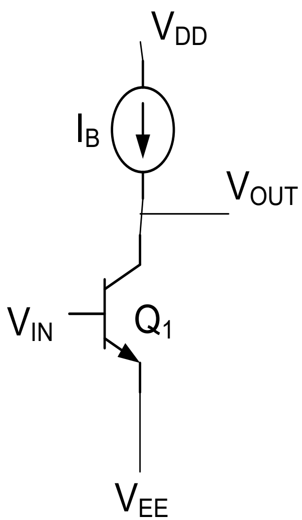
Basic Current Sources and Sinks

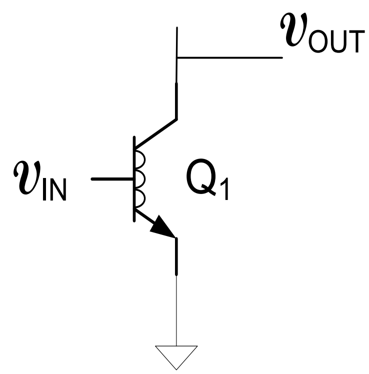
Small-signal Model of MOS Current Sinks and Sources



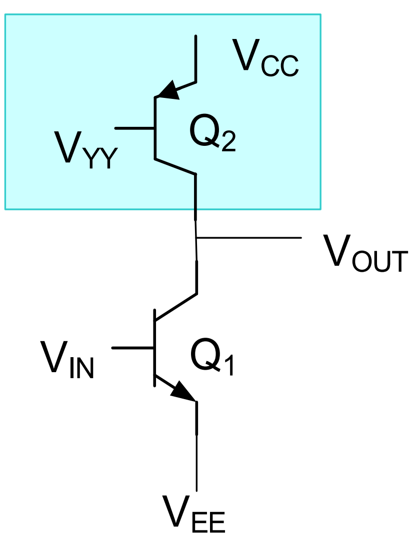
Small-signal model of all other MOS Sinks and Sources introduced thus far are the same

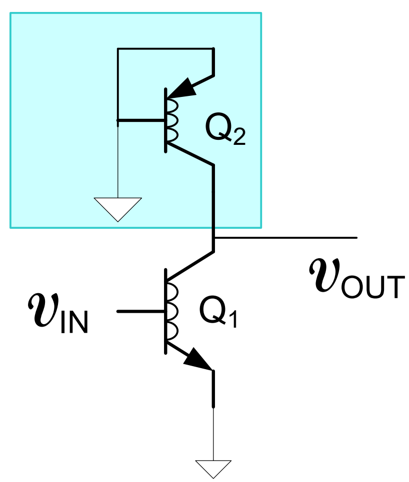
High-gain amplifier

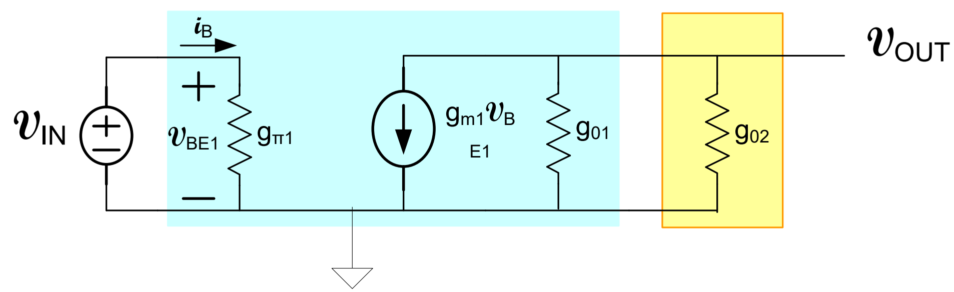




$$A_V = \frac{-g_m}{g_0}$$

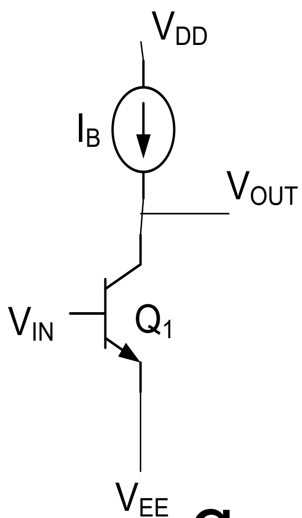




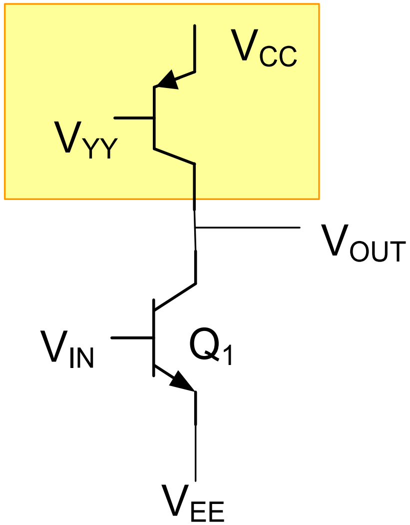


$$A_V = \frac{-g_{m1}}{g_{01} + g_{02}} \cong \frac{-g_{m1}}{2g_{01}}$$

High-gain amplifier



$$\frac{g_m}{g_0} = \frac{g_{m1}}{g_{01}} = \frac{V_{AF}}{V_t} \cong 8000$$



$$A_V = \frac{-g_m}{g_0} = -8000$$

$$A_V \cong \frac{-g_{m1}}{2g_{01}} = -4000$$

- **Nonideal current source decreased the gain by a factor of 2**
- **But the voltage gain is still quite large (-4000)**

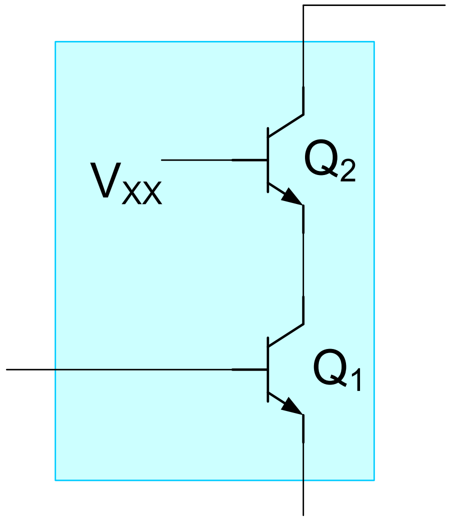
Can the gain be made even larger?

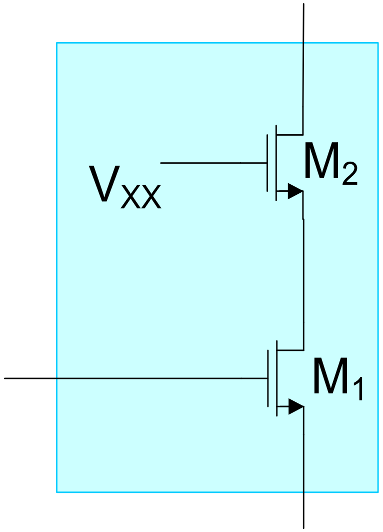
High-gain amplifier

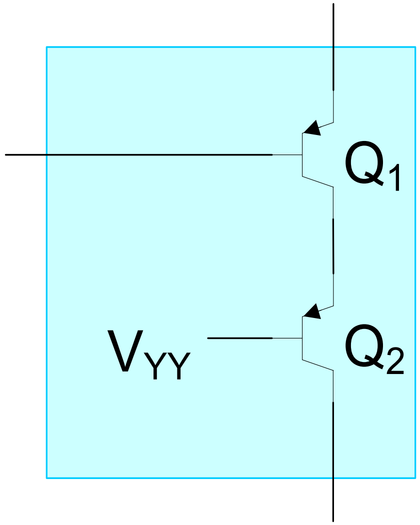
Can the gain be made even larger?

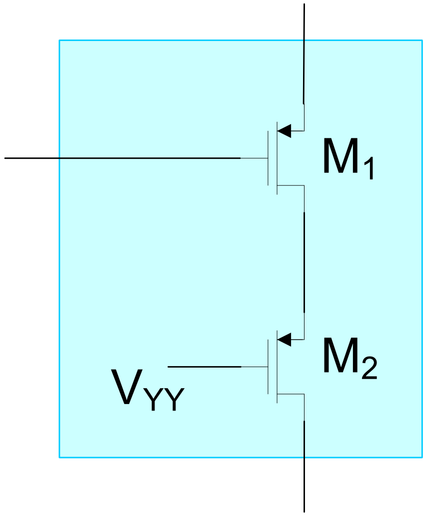
Discuss

The Cascode Configuration

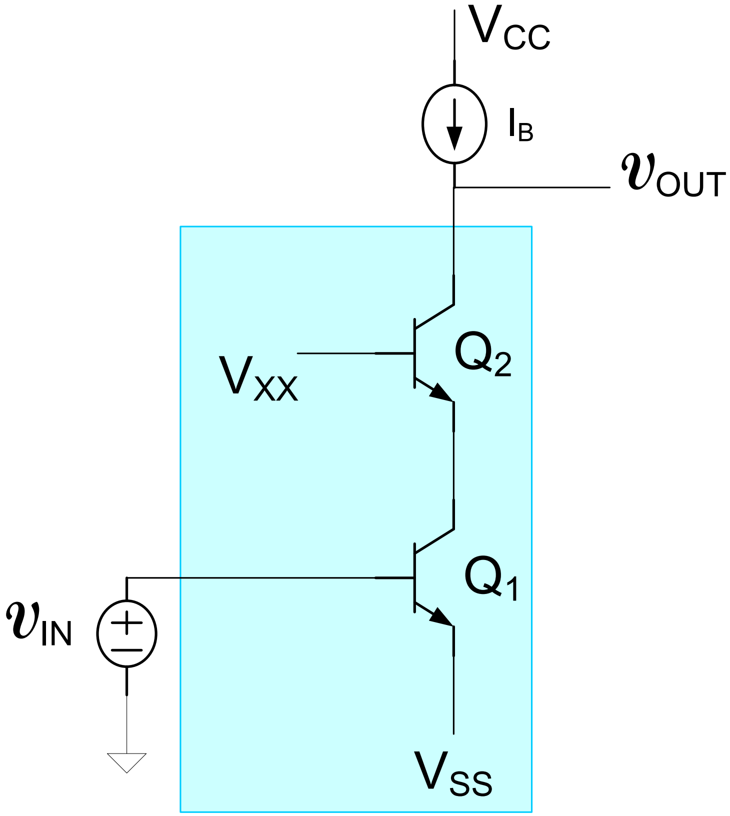








The Cascode Amplifier (consider npn BJT version)



- **Actually a cascade of a CE stage followed by a CB stage but usually viewed as a "single-stage" structure**

- **Cascode structure is widely used**

Basic Amplifier Structures

Discuss

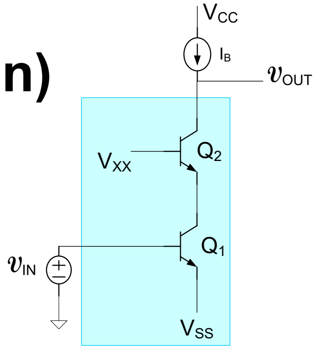
1. Common Emitter/Common Source
2. Common Collector/Common Drain
3. Common Base/Common Gate
4. Common Emitter with R_E/ Common Source with R_S

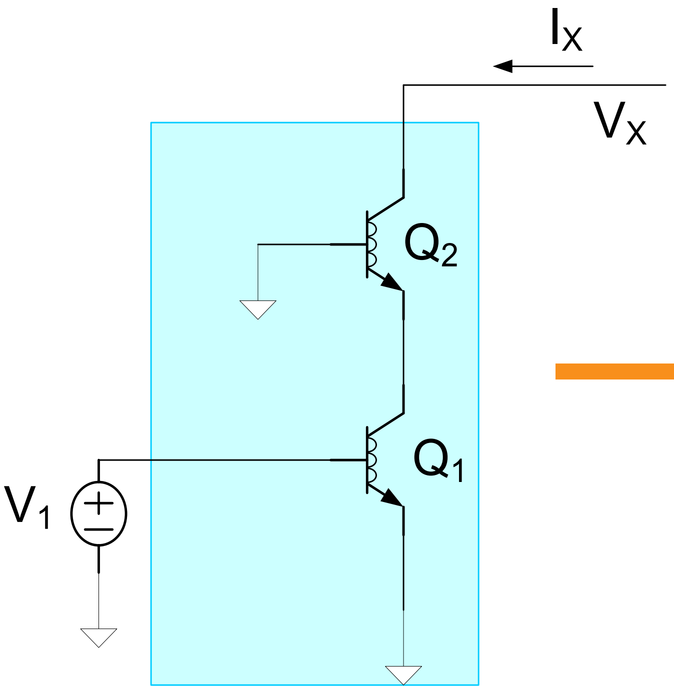
→

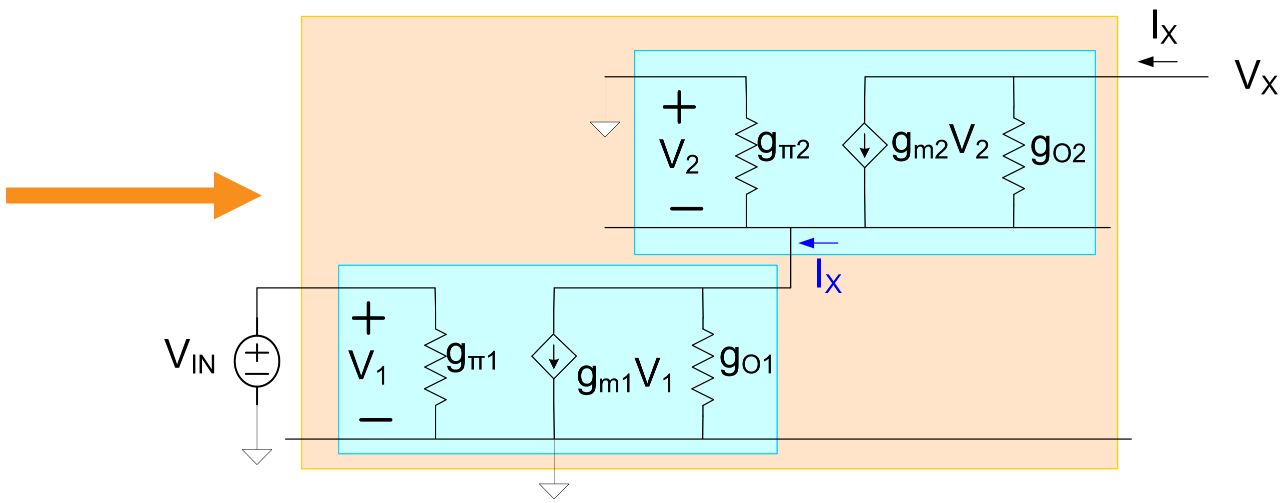
5. Cascode (actually CE:CB or CS:CD cascade)
6. Darlington (special CE:CE or CS:CS cascade)

The first 4 are most popular

The Cascode Amplifier (consider npn BJT version)

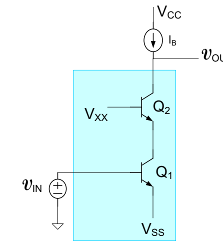


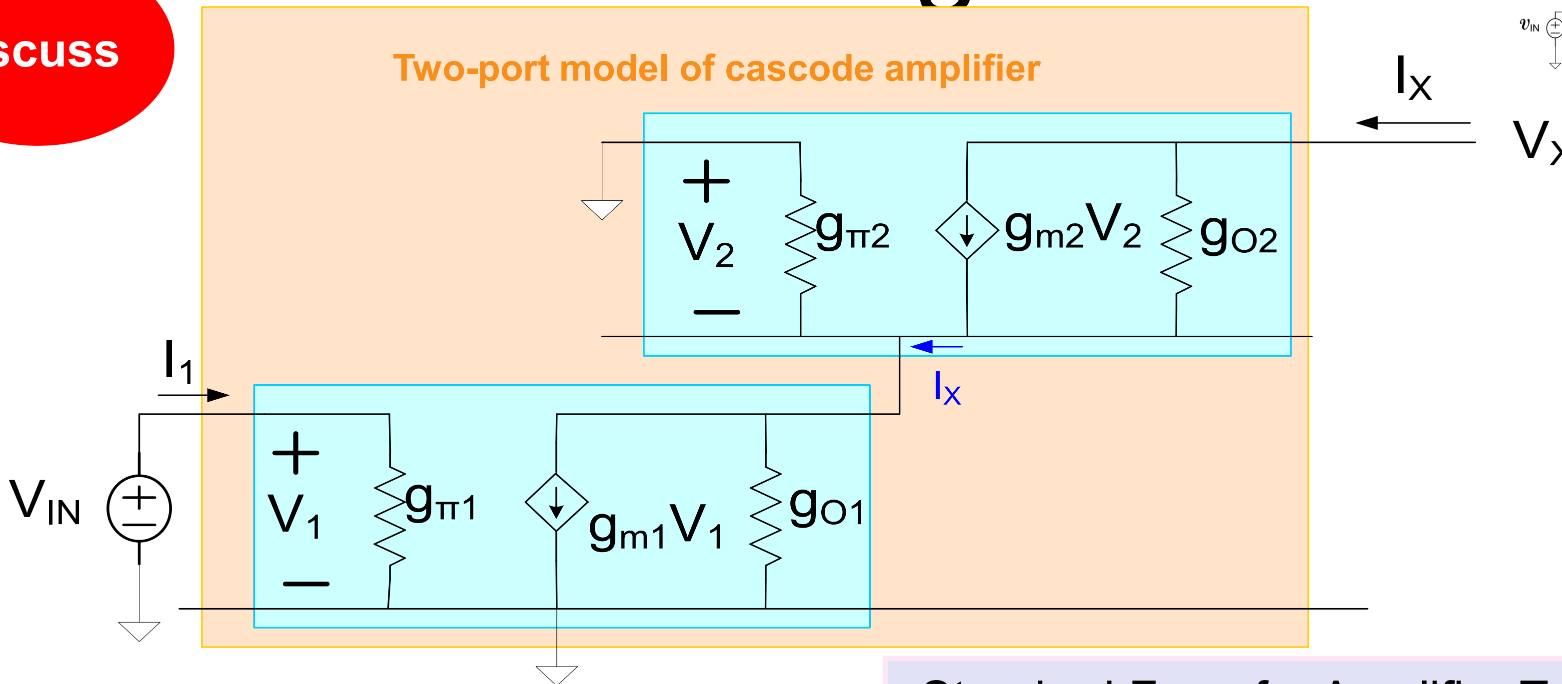




Cascode Configuration

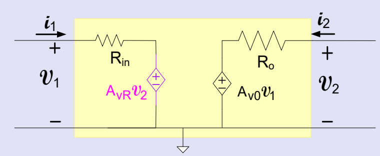
Discuss





$$\left.\begin{aligned}(V_X+V_2)g_{02}+V_2g_{m2}&=I_X\\ V_1\, g_{m1}-V_2(g_{01}+g_{\pi 2})&=I_X\end{aligned}\right\}$$

Standard Form for Amplifier Two-Port



$$v_1 = i_1R_{IN} + A_{VR}v_2$$
$$v_2 = i_2R_O + A_{V0}v_1$$

Observing V_1=V_{IN} and eliminating V_2 between these two equations, we obtain

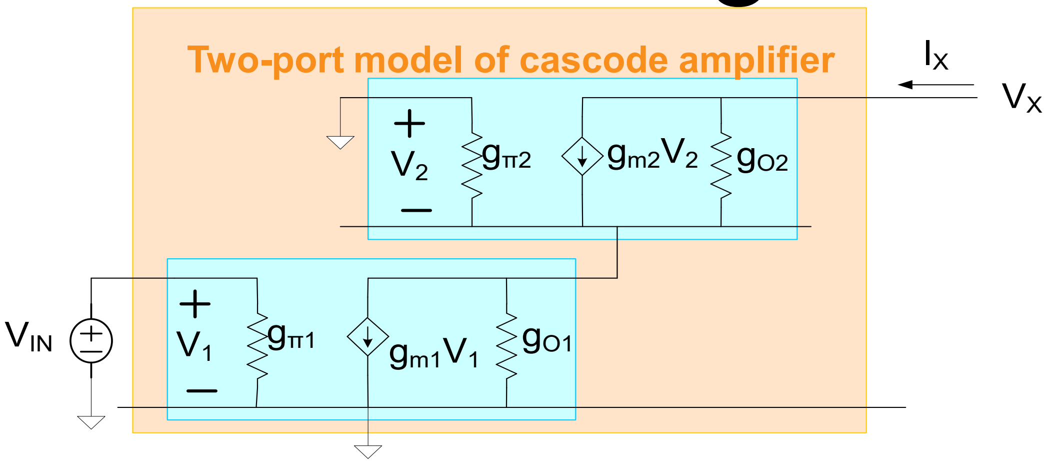
$$V_{IN}=I_1\bullet\frac{1}{g_{\pi 1}}$$

and

$$V_X=I_X\bullet\left[\frac{g_{01}+g_{02}+g_{\pi 2}+g_{m2}}{g_{02}(g_{01}+g_{\pi 2})}\right]-V_{IN}\bullet\left[\frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi 2}+g_{01})}\right]$$

Cascode Configuration

Discuss



$$V_X = I_X \bullet \left[\frac{g_{01}+g_{02}+g_{\pi 2}+g_{m2}}{g_{02}(g_{01}+g_{\pi 2})}\right] - V_{IN} \bullet \left[\frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi 2}+g_{01})}\right]$$

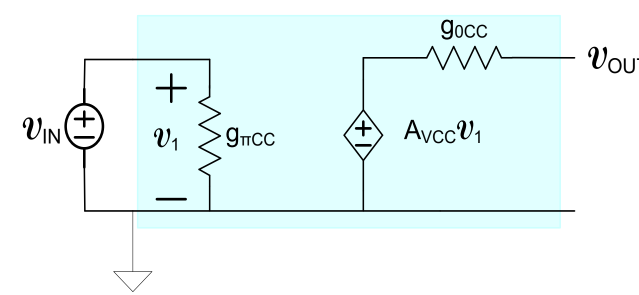
$$V_{IN} = I_1 \bullet \frac{1}{g_{\pi 1}}$$

It thus follows for the npn bipolar structure that :

$$A_{VCC} = -\left[\frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi 2}+g_{01})}\right] \cong -\left[\frac{g_{m1}g_{m2}}{g_{02}g_{\pi 2}}\right]$$

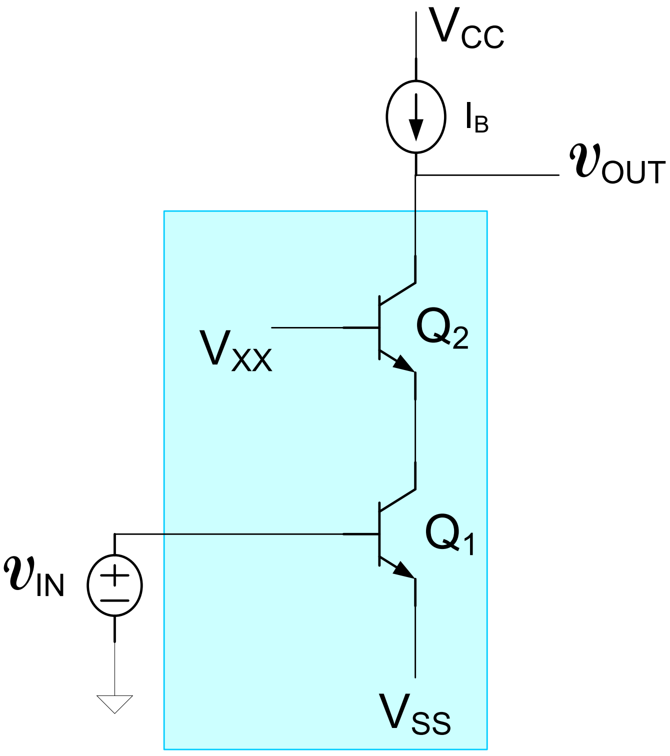
$$g_{0CC} = \left[\frac{g_{02}(g_{01}+g_{\pi 2})}{g_{01}+g_{02}+g_{\pi 2}+g_{m2}}\right] \cong \left[\frac{g_{02}g_{\pi 2}}{g_{m2}}\right]$$

$$g_{\pi CC} = g_{\pi 1}$$



Cascode Configuration

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{02}g_{\pi 2}}\right]$$

$$g_{0CC} \cong \left[\frac{g_{02}g_{\pi 2}}{g_{m2}}\right]$$

$$g_{\pi CC} = g_{\pi 1}$$

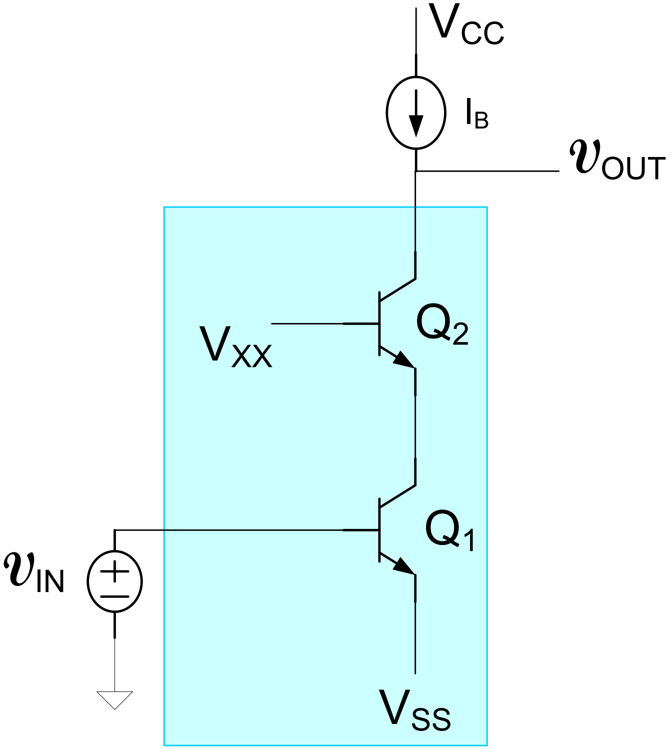
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{02}}\beta\right] \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

- **Voltage gain is a factor of β larger than that of the CE amplifier with current source load**
- **Output impedance is a factor of β larger than that of the CE amplifier**

Cascode Configuration

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{02}}\beta\right] \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$$g_{0CC} \cong \frac{g_{02}}{\beta}$$

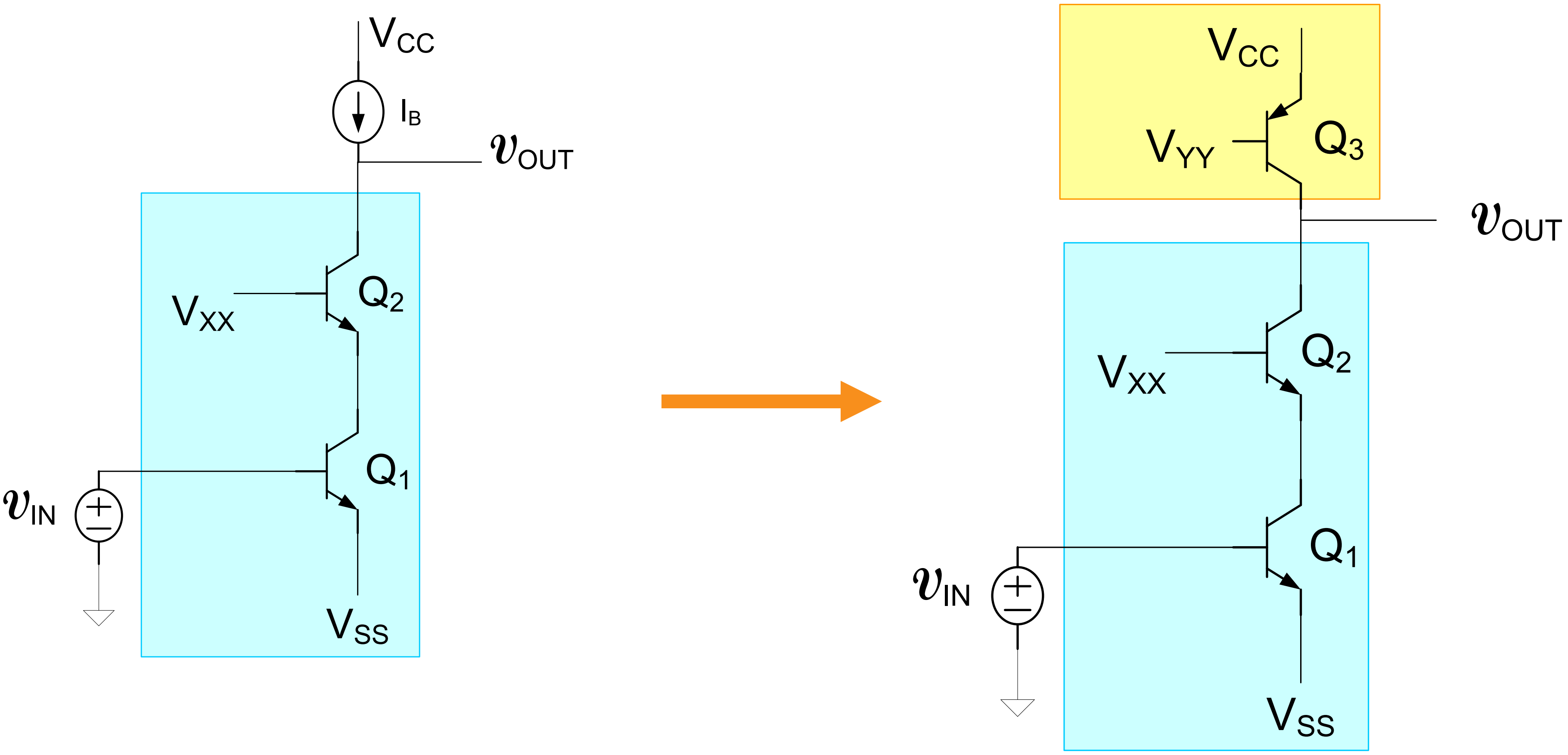
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta = \left[\frac{2V_{AF}}{V_t}\right]\beta = [-8000]100$$

$$A_{VCC} \cong -800{,}000$$

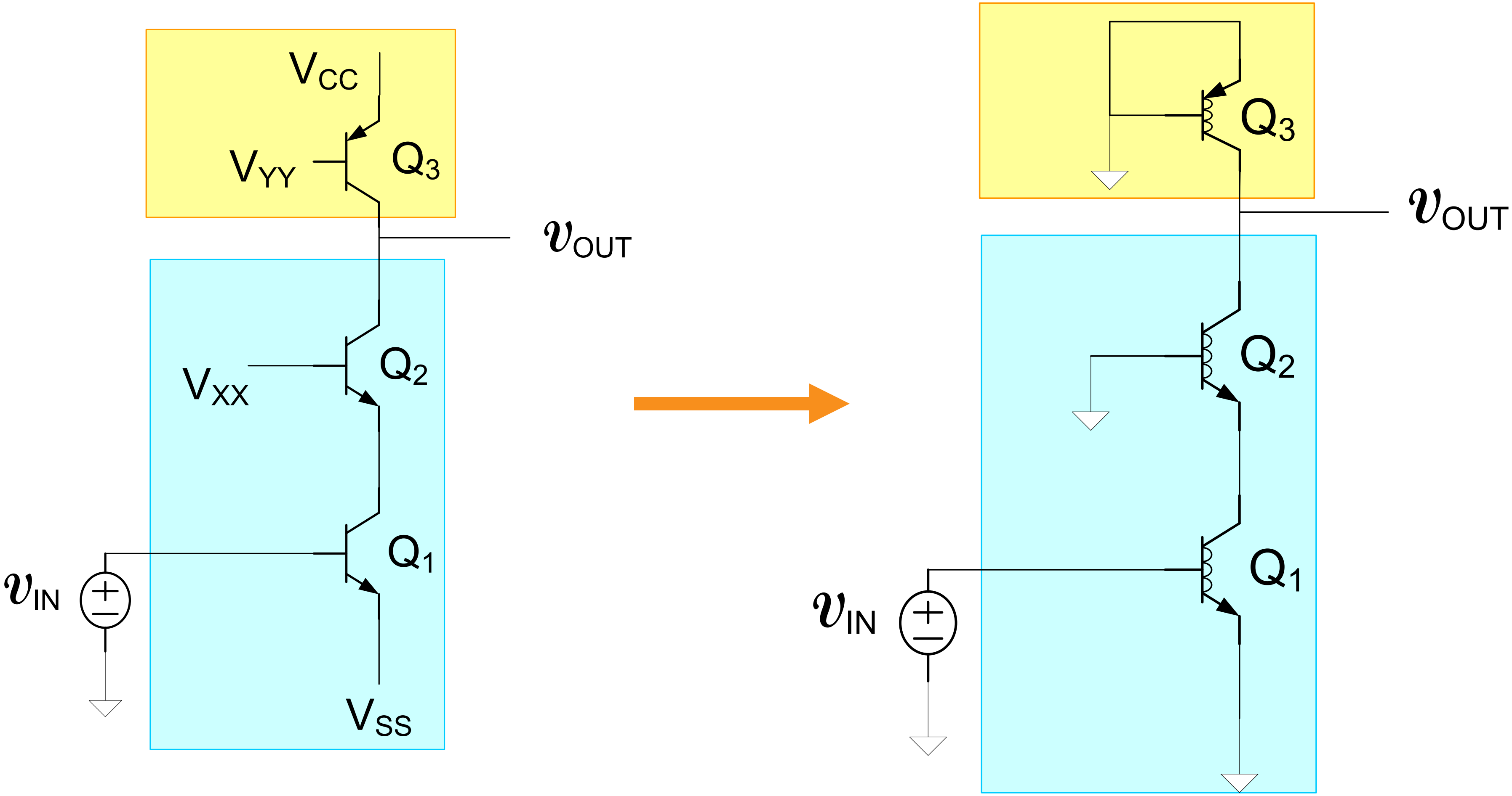
This gain is very large and only requires two transistors!

What happens to the gain if a transistor-level current source is used for I_B?

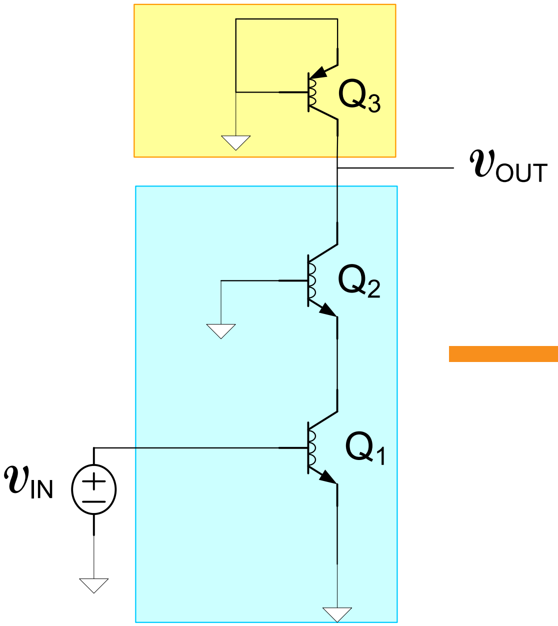
Cascode Configuration

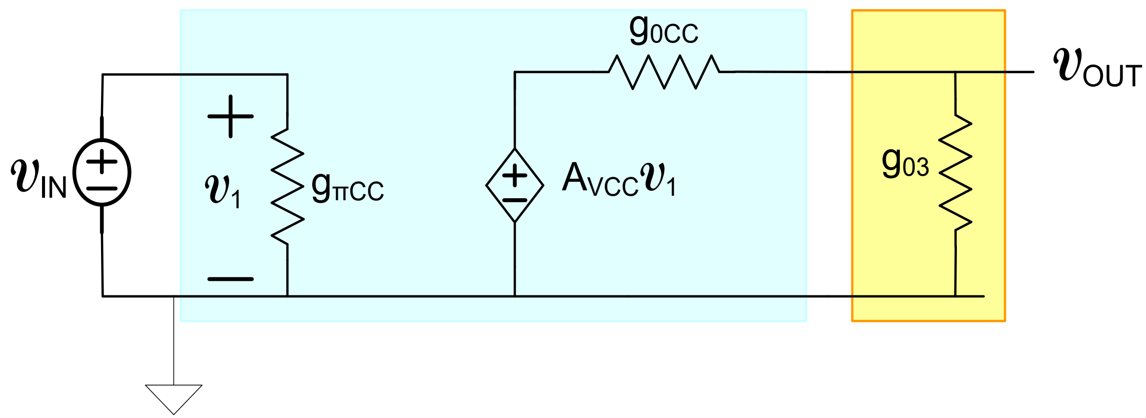


Cascode Configuration



High-gain amplifier comparisons





It thus follows that

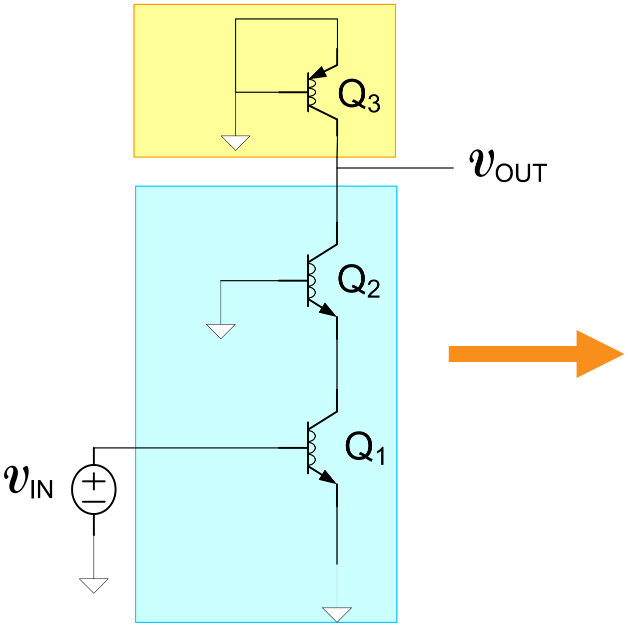
$$A_V = A_{VCC}\left[\frac{g_{0CC}}{g_{03}+g_{0CC}}\right]$$

But $\quad g_{0CC} \simeq g_{01}/\beta = g_{03}/\beta$

$$A_V \cong A_{VCC}\left[\frac{g_{0CC}}{g_{03}}\right] \cong \frac{A_{VCC}}{\beta}$$

This is a dramatic reduction in gain compared to what the ideal current source biasing provided

Cascode Configuration



$$A_V \cong A_{VCC}\left[\frac{g_{0CC}}{g_{03}}\right] \cong \frac{A_{VCC}}{\beta}$$

But recall

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

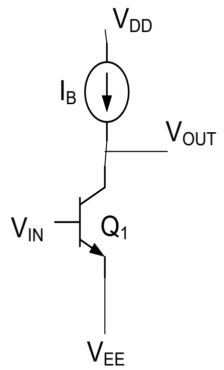
Thus

$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

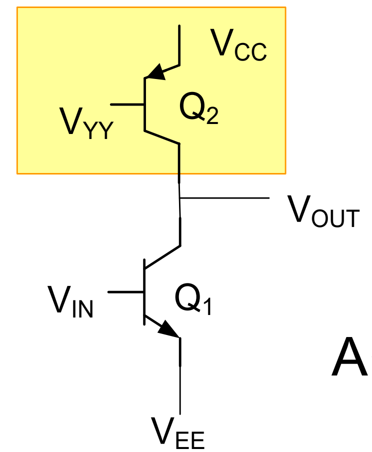
$$A_V \cong -\left[\frac{I_{CQ}/V_t}{I_{CQ}/V_{AF}}\right] = -\left[\frac{V_{AF}}{V_t}\right] \cong -8000$$

- **This is still a factor of 2 better than that of the CE amplifier with transistor current source** $\left(A_{VCE} \cong -\left[\frac{g_{m1}}{2g_{01}}\right]\right)$
- **It only requires one additional transistor**
- **But its not nearly as good as the gain the cascode circuit seemed to provide**

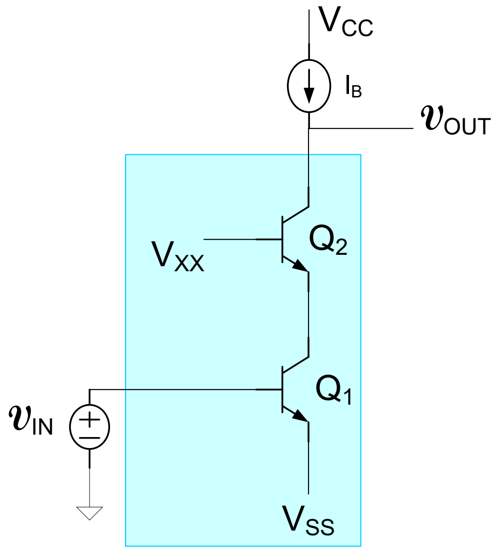
Cascode Configuration Comparisons



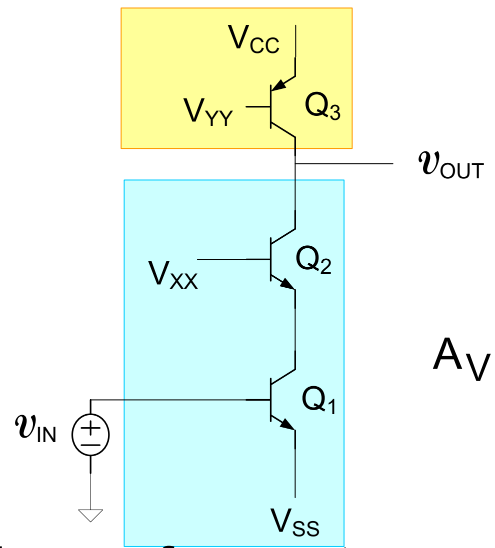
$$A_V = \frac{-g_m}{g_0}$$



$$A_V \cong \frac{-g_{m1}}{g_{01} + g_{02}} = \frac{-g_{m1}}{2g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



$$A_V \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta} + g_{03}}\right] \cong -\left[\frac{g_{m1}}{g_{03}}\right]$$

Gain limited by output impedance of current scource !!

Can we design a better current source?

In particular, one with a higher output impedance?

Better current sources

Need a higher output impedance than g_o

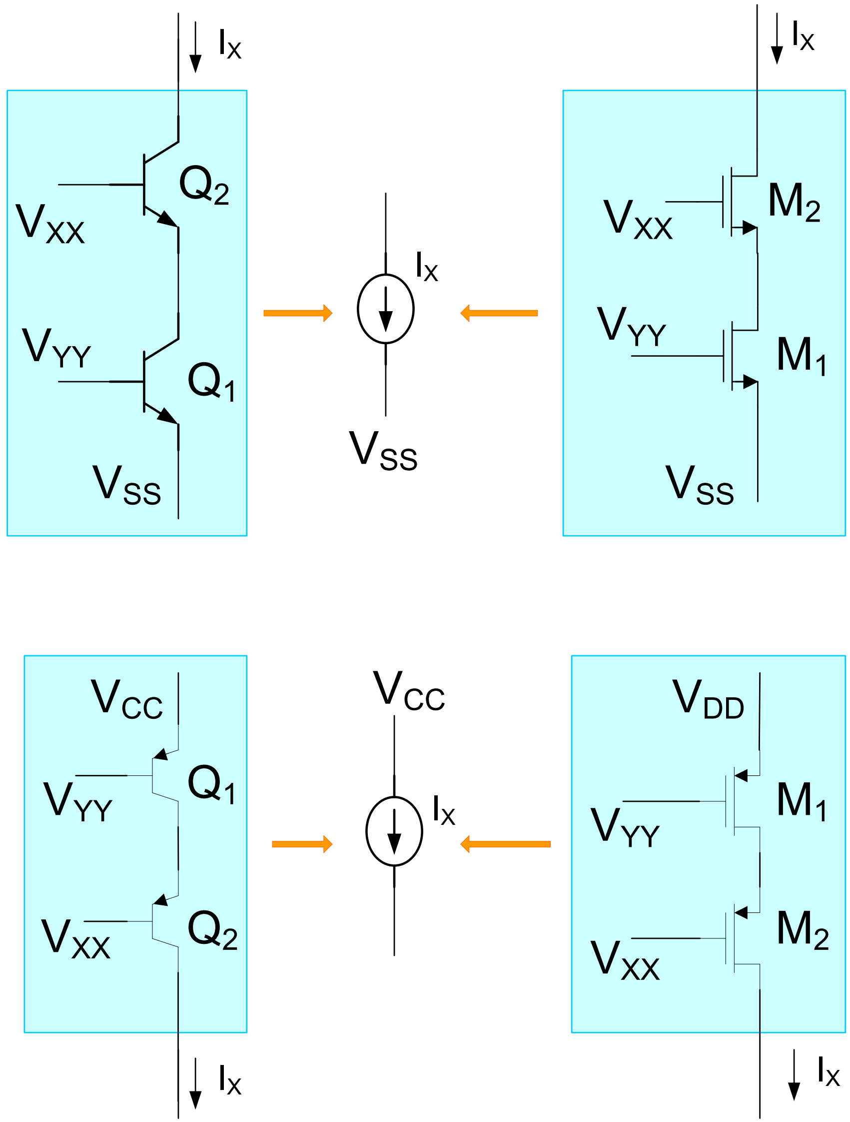
The output impedance of the cascode circuit itself was very large !

$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

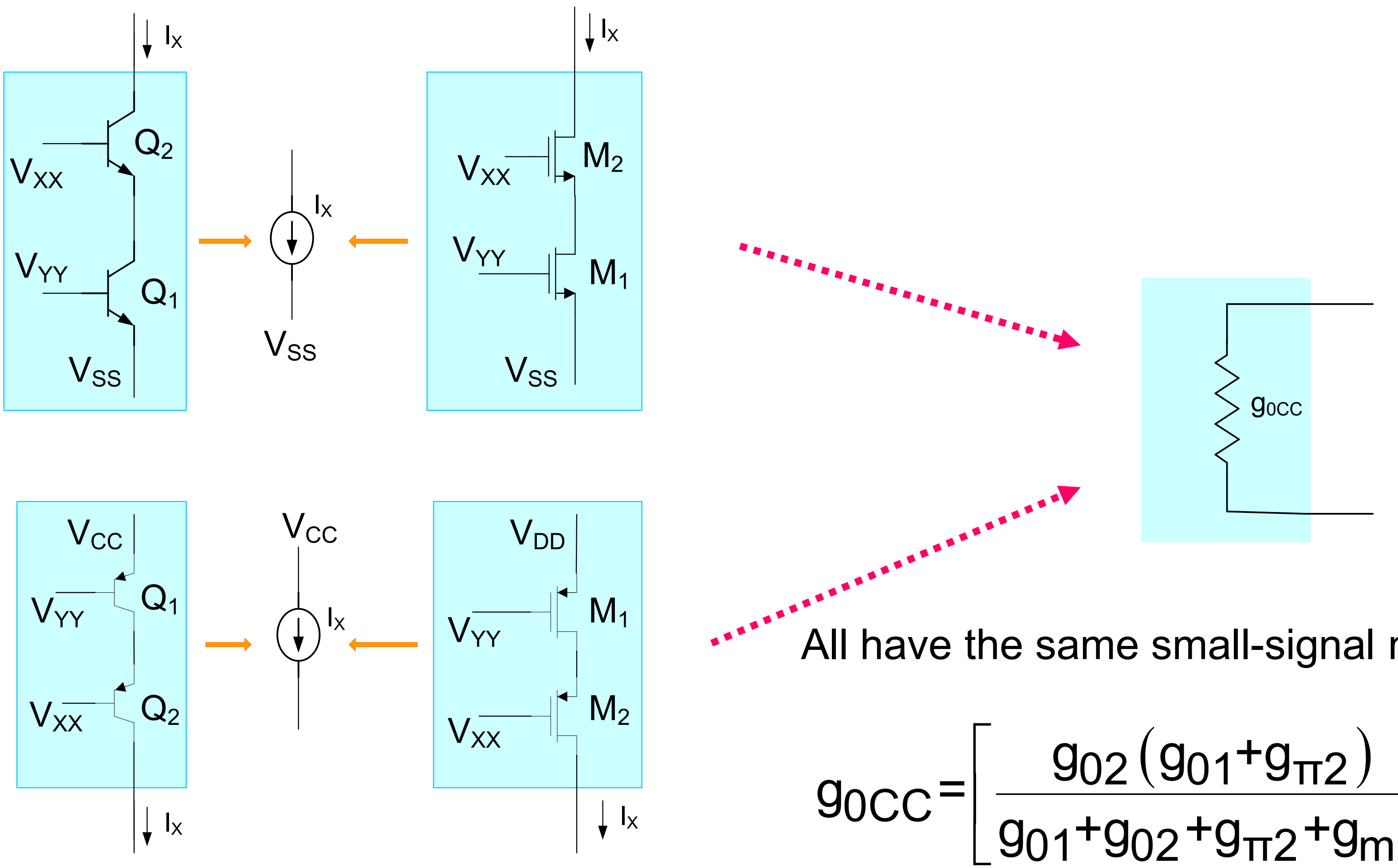
Can a current source be built with the cascode circuit ?

Cascode current sources

Discuss



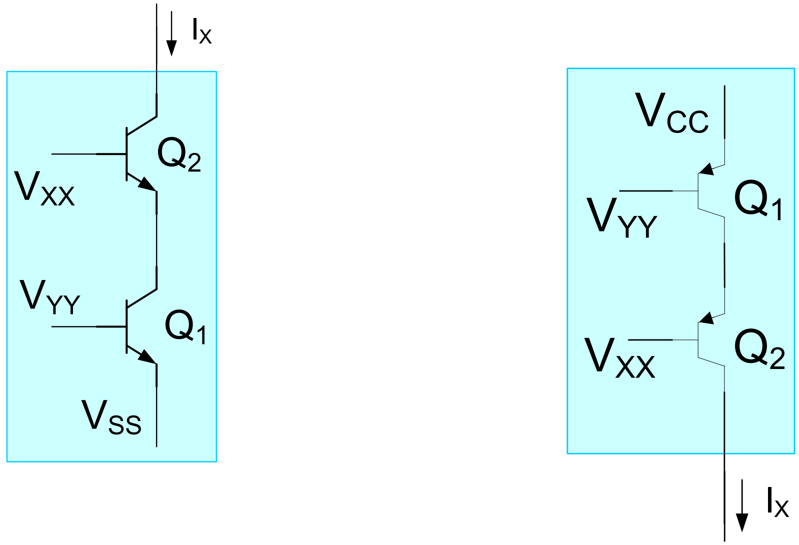
Cascode current sources



All have the same small-signal model

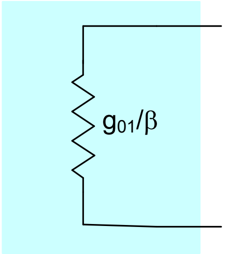
$$g_{0CC} = \left[\frac{g_{02}\left(g_{01} + g_{\pi 2}\right)}{g_{01} + g_{02} + g_{\pi 2} + g_{m2}} \right]$$

Cascode current sources

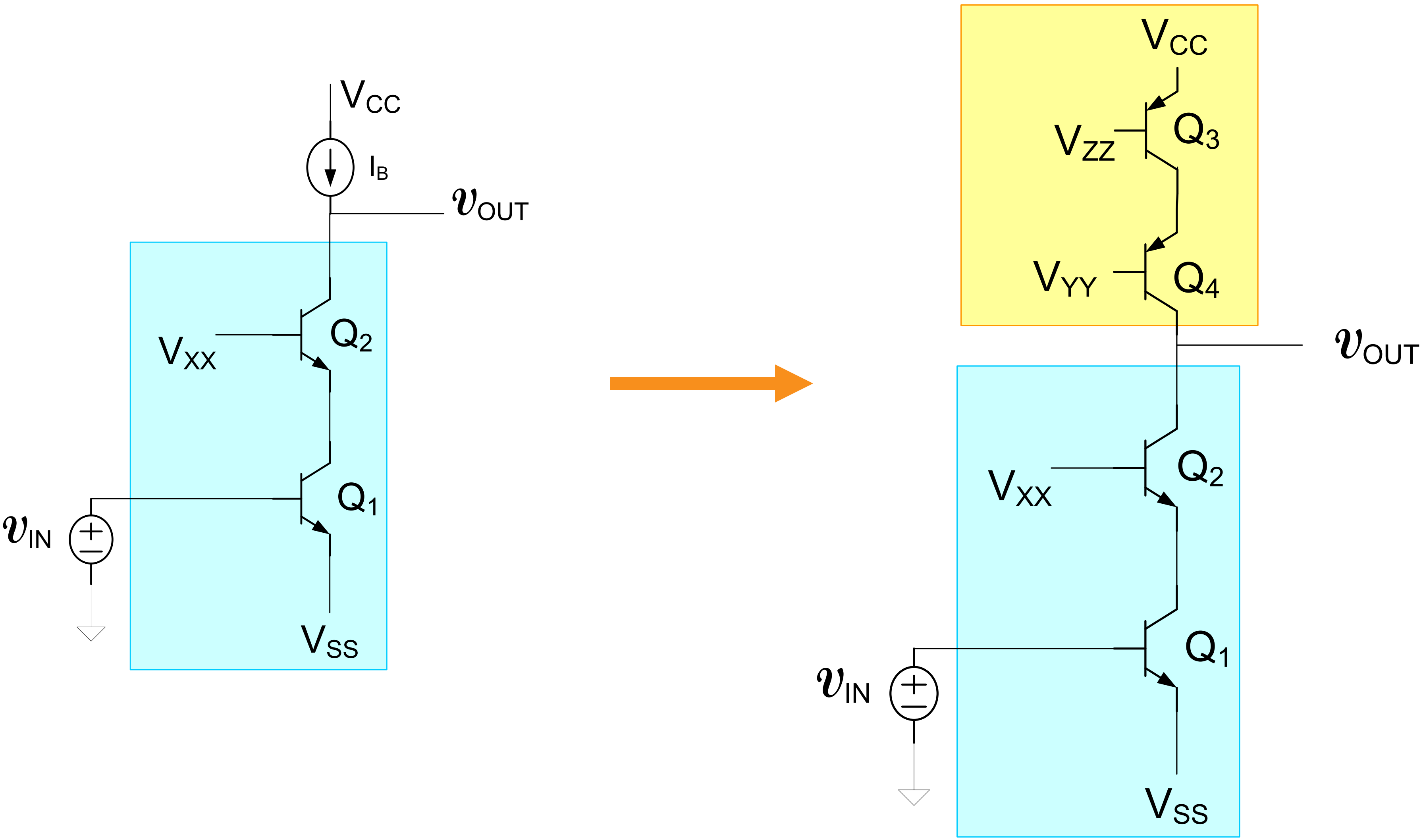


For the BJT cascode current sources

$$g_{0CC} = \left[\frac{g_{02}\left(g_{01}+g_{\pi 2}\right)}{g_{01}+g_{02}+g_{\pi 2}+g_{m2}} \right] \cong \left[\frac{g_{02}g_{\pi 2}}{g_{m2}} \right] = \frac{g_{01}}{\beta}$$

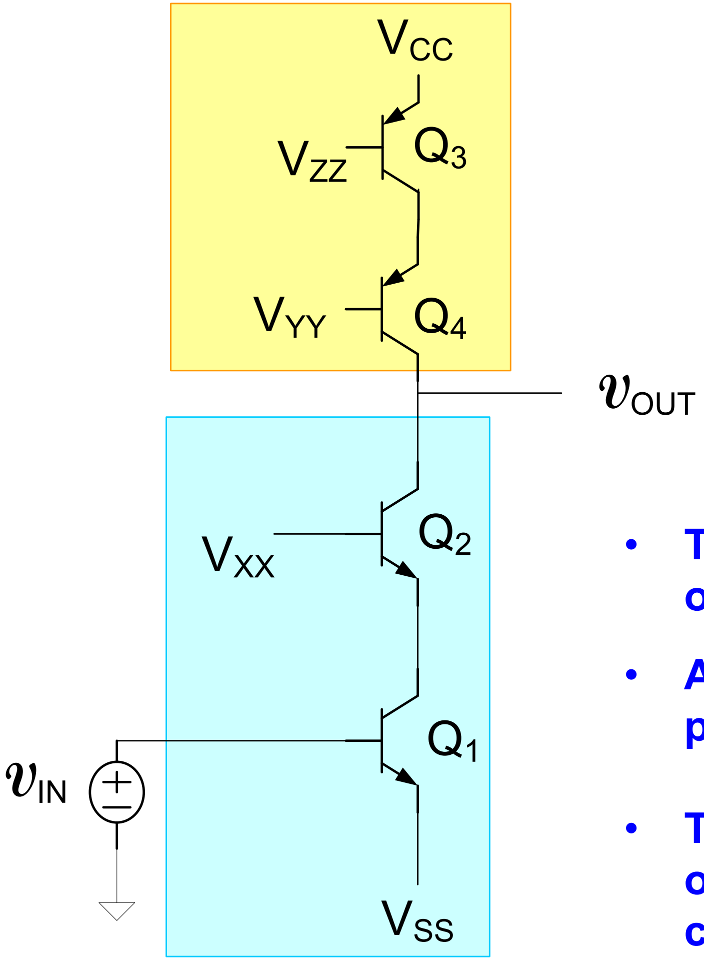


Cascode Configuration



Cascode Configuration

Discuss



$$A_V \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta_1}+g_{0CC}}\right] \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta_1}+\frac{g_{03}}{\beta_3}}\right]$$

If $\beta_1=\beta_3=\beta$

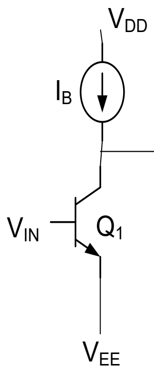
$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

$$A_V = -[8000]\frac{100}{2} \cong -400{,}000$$

- **This gain is very large and is a factor of 2 below that obtained with an ideal current source biasing**
- **Although the factor of 2 is not desired, the performance of this circuit is still very good**
- **This factor of 2 gain reduction is that same as was observed for the CE amplifier when a transistor-level current source was used**
- **Biasing voltages V_{ZZ} and V_{SS} are critical so seldom used single-ended but good biasing strategies exist for differential operation**

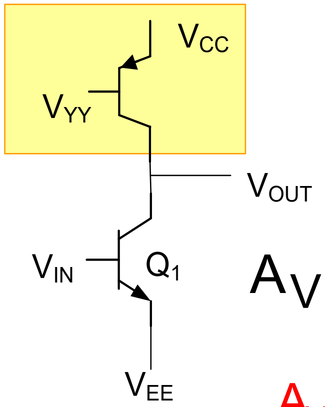
Cascode Configuration Comparisons

Discuss



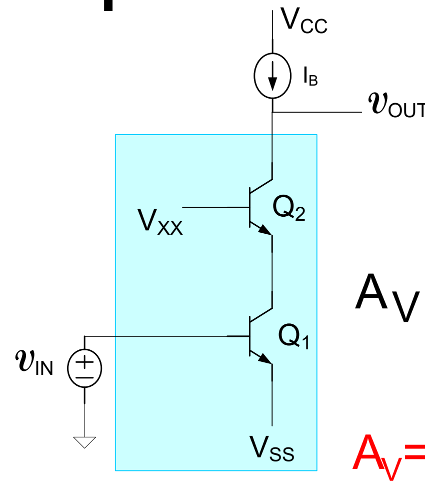
$$A_V = \frac{-g_m}{g_0}$$

$A_V = -8{,}000$



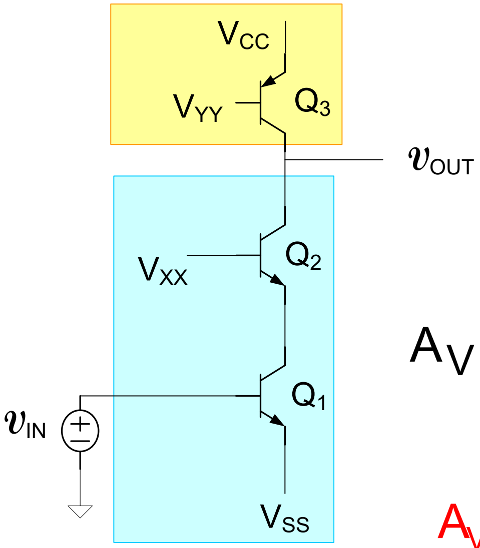
$$A_V \cong \frac{-g_{m1}}{2g_{01}}$$

$A_V = -4{,}000$



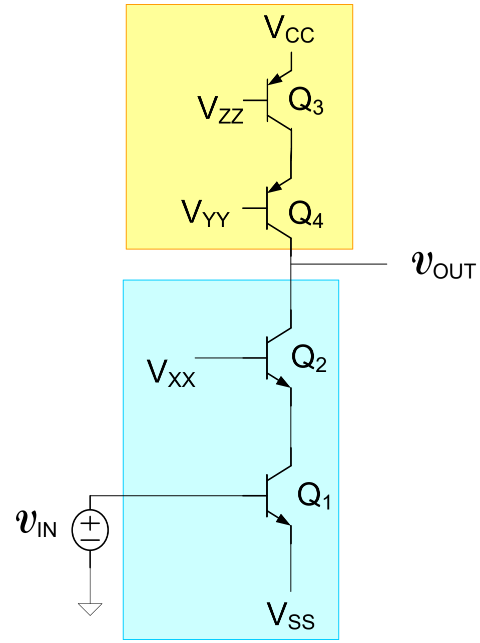
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$A_V = -800{,}000$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

$A_V = -8{,}000$

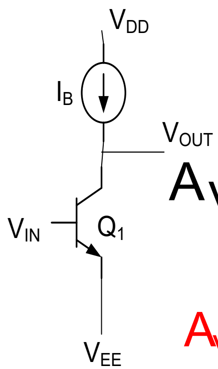


$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

$A_V = -400{,}000$

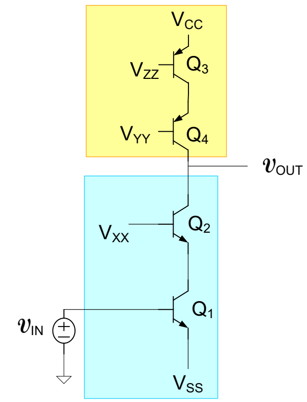
Can we use more cascoding to further increase the gain?

High Gain Amplifiers Seldom Used Open Loop



$$A_V = \frac{-g_m}{g_0}$$

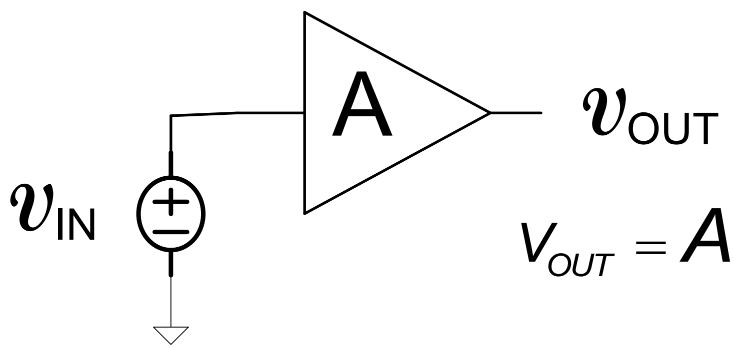
$A_V = -8{,}000$



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

Discuss

$A_V = -400{,}000$



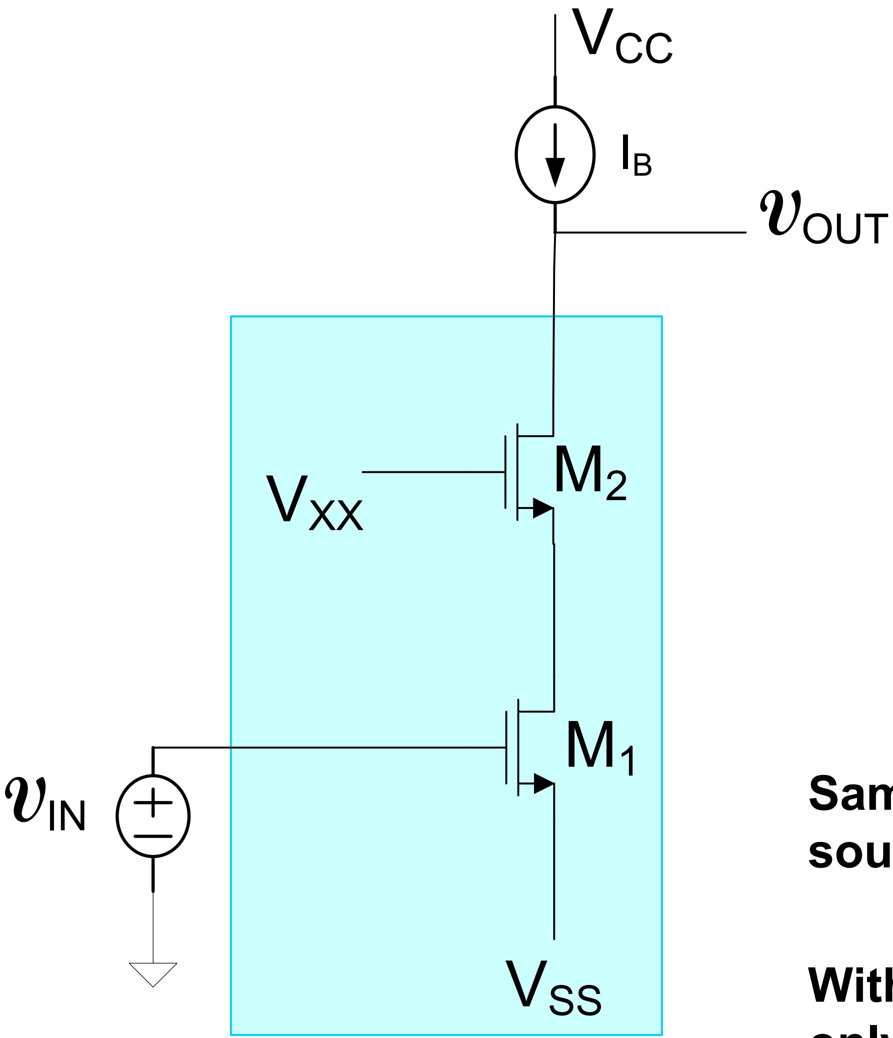
$$V_{OUT} = A\,v_{IN} + V_{OUTQ}$$

If A_V=-400,000 and V_{IN} increases by 1mV, what would happen at the output?

$|V_{OUT}|$ would increase by 400,000 x 1mV=-400V

The Cascode Amplifier (consider n-ch MOS version)

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1} g_{m2}}{g_{01} g_{02}}\right]$$

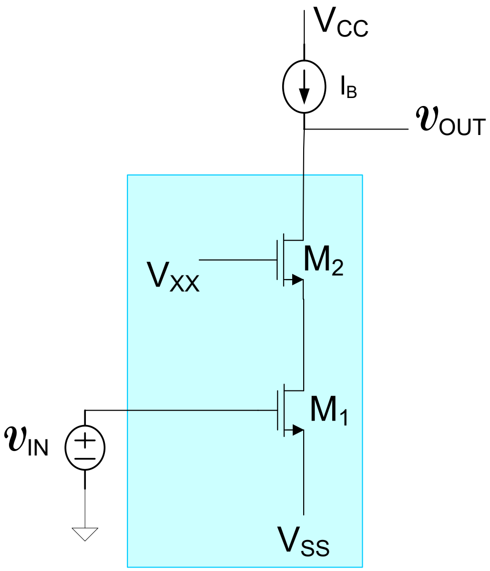
$$g_{0CC} \cong \left[\frac{g_{01} g_{02}}{g_{m2}}\right]$$

Same issues for biasing with current source as for BJT case

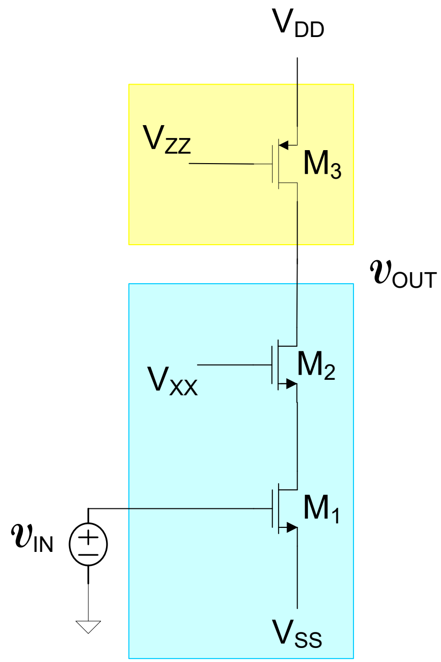
With cascode current source for I_B, gain only drops by a factor of 2 from value with ideal current source

The Cascode Amplifier (consider n-ch MOS version)

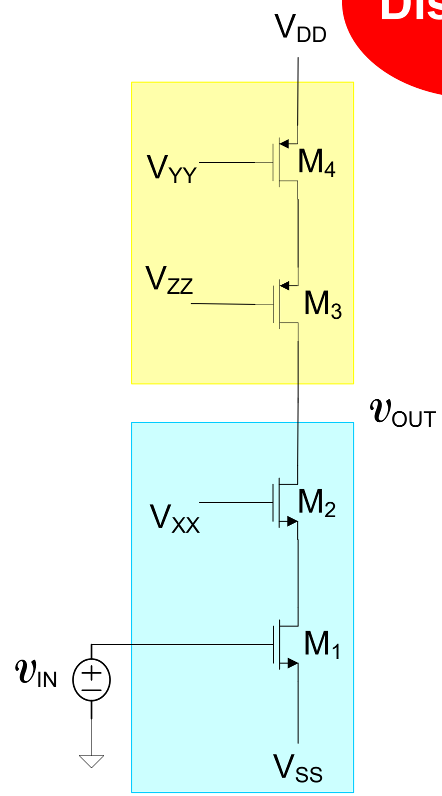
Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$



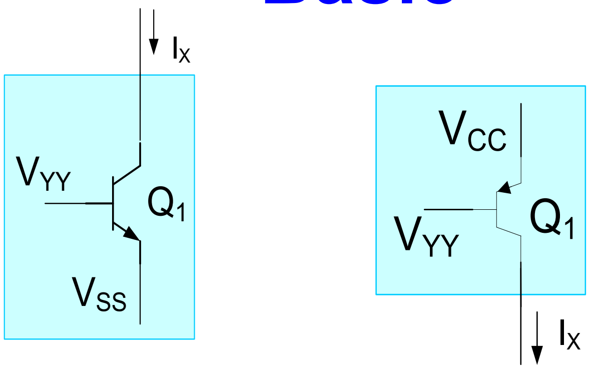
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

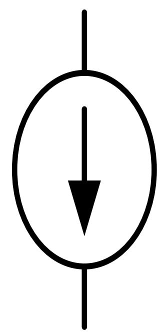


$$A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

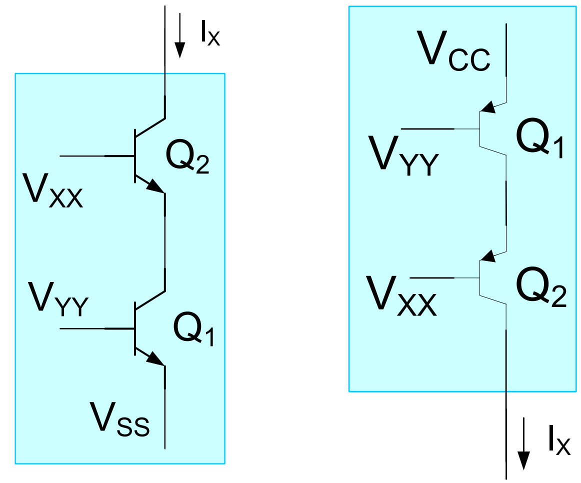
Current Source Summary (BJT)

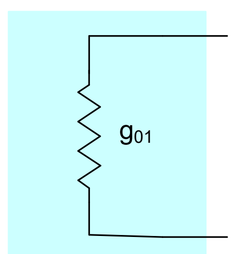
Basic



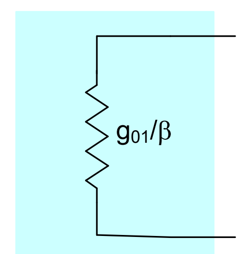


Cascode





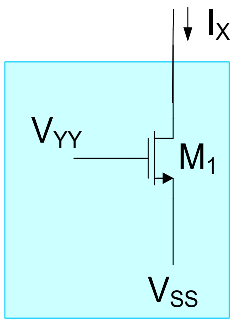
$$g_0 \cong g_{01}$$

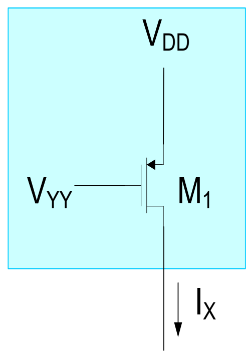


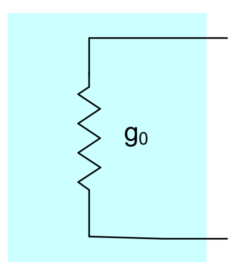
$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

Current Source Summary (MOS)

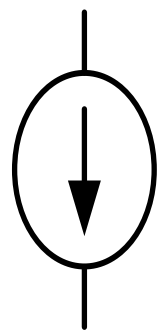
Basic



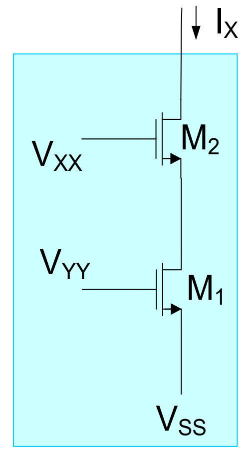


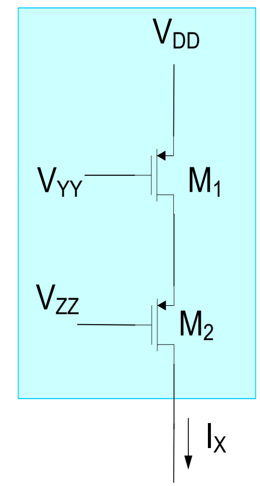


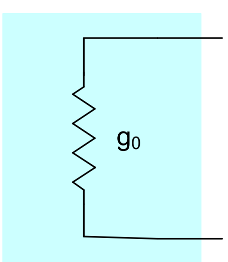
$$g_0 \cong g_{01}$$



Cascode

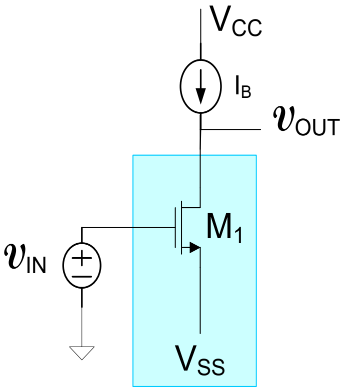




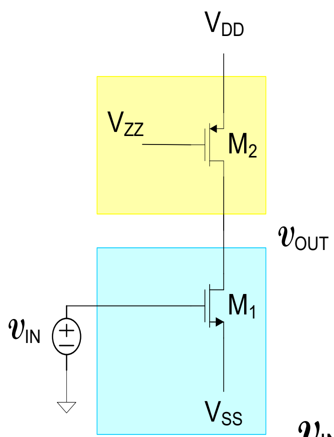


$$g_0 \cong g_{01}\frac{g_{02}}{g_{m2}}$$

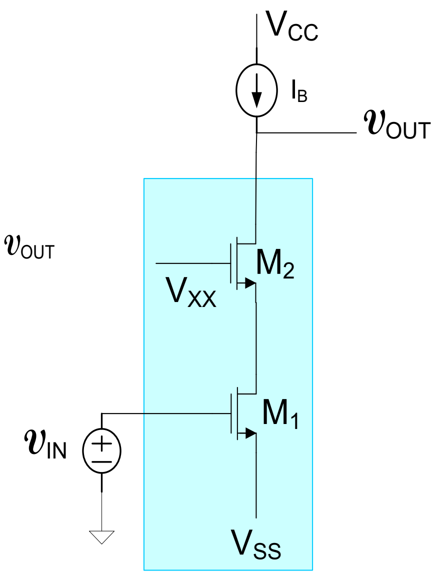
High Gain Amplifier Comparisons (n-ch MOS)



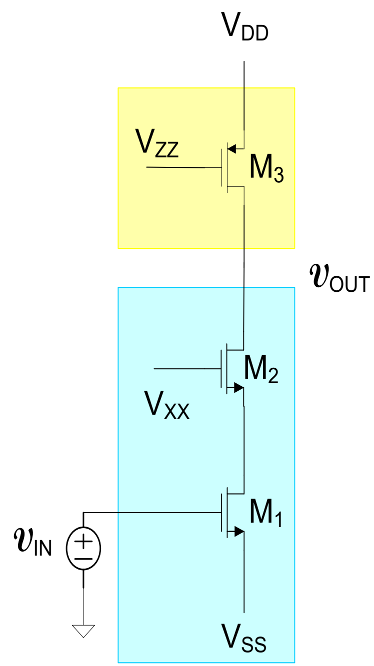
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



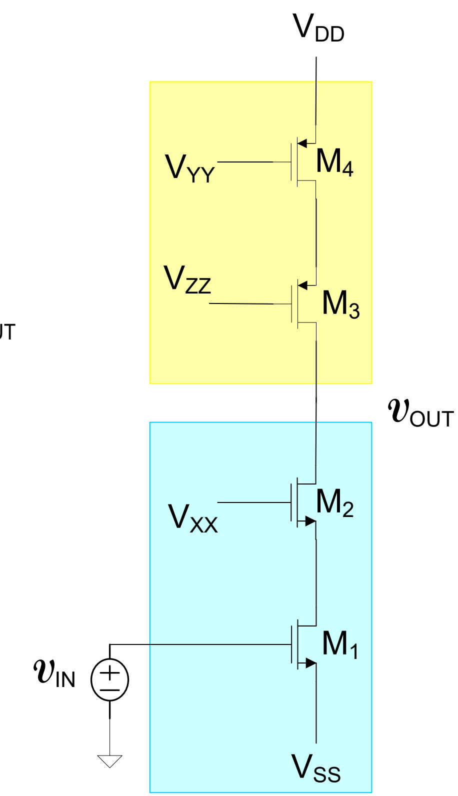
$$A_V \cong -\frac{1}{2}\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

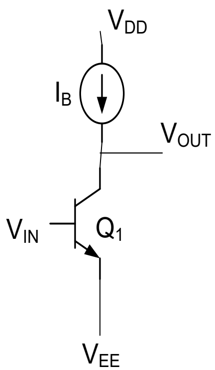


$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

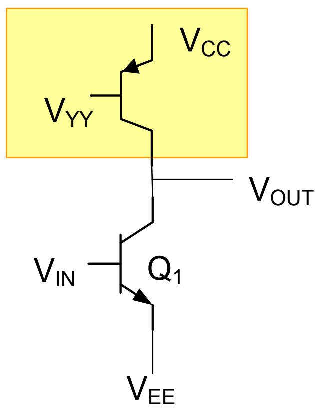


$$A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

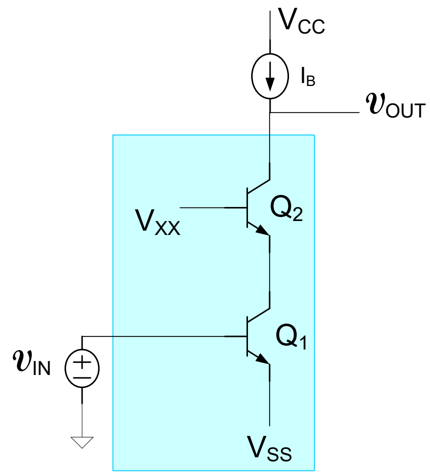
High Gain Amplifier Comparisons (BJT)



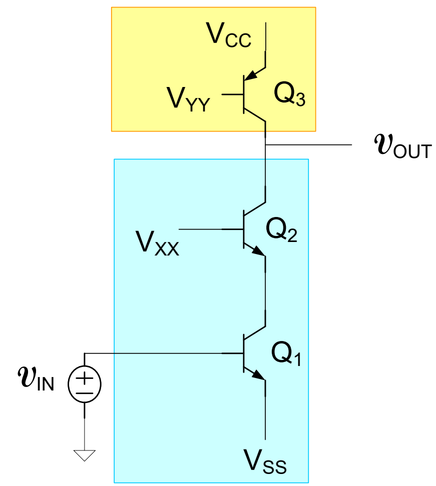
$$A_V = \frac{-g_m}{g_0}$$



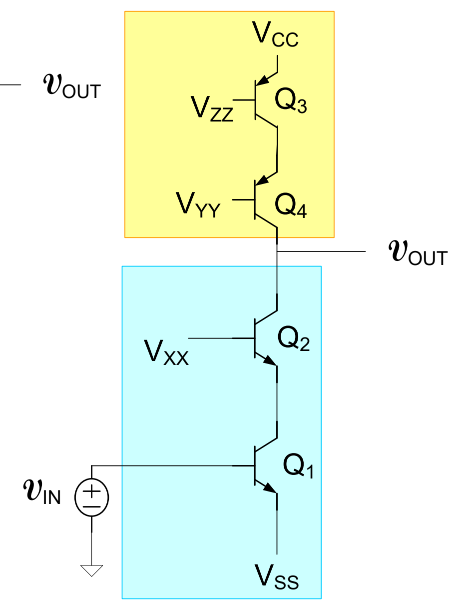
$$A_V \cong -\frac{1}{2}\frac{g_{m1}}{g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

- Single-ended high-gain amplifiers inherently difficult to bias (because of the high gain)
- Biasing becomes practical when used in differential applications
- These structures are widely used but usually with differential inputs

Stay Safe and Stay Healthy !

End of Lecture 34